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A Generalization of Tutte's Characterization of Totally Unimodular Matrices

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We characterize the symmetric (0, 1)-matrices that can be signed symmetrically so that every principal submatrix has determinant 0, ± 1. This characterization generalizes Tutte's famous characterization of totally unimodular matrices. The result can be viewed as an excluded minor theorem for an interesting class of delta-matroids. © 1997 Academic Press

1. INTRODUCTION

An integral square matrix A is called *principally unimodular* (PU if every nonsingular principal submatrix is unimodular (that is, has determinant ± 1). Principal unimodularity was originally studied with regard to skew-symmetric matrices; see [2, 4, 5]; here we consider symmetric matrices. Our main theorem is a generalization of Tutte's excluded minor characterization of totally unimodular matrices; the generalization arises in the following way: a matrix B is totally unimodular if and only if the matrix $\left(\begin{array}{c|c} 0 & B \\ \hline B^T & 0 \end{array}\right)$ is PU. Before stating the main theorem we need to introduce some terminology.

A *signing* of a symmetric (0, 1)-matrix $A=(a_{ij})$ is a symmetric $(0, \pm 1)$-matrix, say $A'=(a'_{ij})$, such that $a_{ij}=|a'_{ij}|$, for all i, j. We are concerned with the symmetric (0, 1)-matrices that admit a signing which is PU; such a signing is called a PU-*signing*. Let A be a V by V matrix, where V is a finite set. An *isomorphism* of A is a matrix obtained from A by a relabeling of its ground set V. (Note that isomorphisms freely allow simultaneous row-column exchanges.) We denote by $A[X]$ the principal submatrix of A induced by the set $X\subseteq V$. For a set $X\subseteq V$ such that $A[X]$ is nonsingular, define matrices P, Q, R, S, such that $P=A[X]$ and $A=\left(\begin{array}{c|c} P & Q \\ \hline R & S \end{array}\right)$. Then define

$$A * X=\left(\begin{array}{c|c} -P^{-1} & P^{-1}Q \\ \hline RP^{-1} & S-RP^{-1}Q \end{array}\right).$$

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We refer to this operation as a *pivot*; we are interested in pivoting over the reals and also over $GF(2)$. We denote the pivot $A * X$ performed over $GF(2)$ by $A \times X$, and we call this *a binary pivot*. Note that if A is symmetric then $A * Y$ is also symmetric. Let A and B be symmetric $(0, 1)$-matrices. If there exists a nonsingular, principal submatrix $A[X]$ of A such that B is isomorphic to a principal submatrix of $A \times X$, then we say that A *reduces to* B. The main result of this paper is the following.

THEOREM 1.1. *Let A be a symmetric $(0, 1)$-matrix. A has no PU-signing if and only if A reduces to one of the matrices $B_1, ..., B_5$ (defined in Fig. 1).*

(Figure 2 depicts the matrices $B_1, ..., B_5$ graphically.) Let A and A' be symmetric matrices such that A reduces to A'. If, for some matrix B, $A = \left(\begin{array}{c|c} 0 & B \\ B^T & 0 \end{array}\right)$, then there exists a matrix B' such that $A' = \left(\begin{array}{c|c} 0 & B' \\ B'^T & 0 \end{array}\right)$. Therefore, as a corollary of Theorem 1.1, we obtain Tutte's excluded minor characterization of totally unimodular matrices.

COROLLARY 1.2 (Tutte [11, 12]). *Let B be a $(0, 1)$-matrix, and let $A = \left(\begin{array}{c|c} 0 & B \\ B^T & 0 \end{array}\right)$. B cannot be signed to be totally unimodular if and only if A reduces to B_5.*

To prove our result, we consider the class of matrices that do not reduce to B_1, and then we use a Theorem of Truemper [10] on beta-balanced matrices which gives us the general form of the matrices that do not admit PU-signings. Our original proof of Theorem 1.1 generalized Gerards [9] short proof of Tutte's theorem. By using Truemper's theorem we simplify the final case analysis.

$$B_1 = \begin{pmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{pmatrix} \qquad B_2 = \left(\begin{array}{c|cccc} 1 & 1 & 1 & 1 & 1 \\ \hline 1 & 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 & 0 \\ 1 & 0 & 1 & 1 & 1 \\ 1 & 1 & 0 & 1 & 1 \end{array}\right)$$

$$B_3 = \left(\begin{array}{ccc|ccc} 1 & 1 & 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 & 0 & 1 \\ \hline 1 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 & 1 \end{array}\right) \qquad B_4 = \left(\begin{array}{ccc|ccc} 1 & 1 & 1 & 0 & 1 & 1 \\ 1 & 1 & 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 & 1 & 0 \\ \hline 0 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 \end{array}\right)$$

$$B_5 = \left(\begin{array}{ccc|cccc} 0 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 0 & 1 \\ \hline 0 & 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 0 \end{array}\right)$$

FIG. 1. Excluded principal submatrices.

2. PRELIMINARIES

Pivoting on principal submatrices was introduced with regard to the linear complementarity problem (see Cottle, Pang, and Stone [8]). Let A be a V by V matrix, that is, a square matrix whose rows and columns are both indexed by the set V Cottle *et al* [8, p. 71] define an operation on a nonsingular principal submatrix $A[X]$, that differs from $A * X$ only by negating the columns indexed by X. (Their operation does not preserve symmetry.)

THEOREM 2.1 (See Cottle *et al.* [8, p. 230]). *Let $A[X]$ be a nonsingular principal submatrix of a V by V matrix A. Then, for $Y \subseteq V$,*

$$\det(A * X[Y]) = \pm \det(A[X \Delta Y])/\det(A[X]).$$

Let A and B be symmetric $(0, 1)$-matrices such that A reduces to B. Suppose that A' is a PU-signing of A. Since A reduces to B, there exists a principal submatrix $A[X]$ of A that is nonsingular over $GF(2)$, and B is isomorphic to a principal submatrix of $A \times X$. Since $A[X]$ is nonsingular over $GF(2)$, $\det(A'[X]) \equiv 1$, modulo 2; hence $A'[X]$ is nonsingular over the reals. By Theorem 2.1, $A' * X$ is PU, and $A' * X$ is a signing of $A \times X$. However, since $A' * X$ is PU, every principal submatrix of $A' * X$ is PU, in particular, B has a PU-signing. Therefore, the family of symmetric matrices that admit PU-signings is closed under reduction. Then proving that $B_1, ..., B_5$ do not admit PU-signings proves Theorem 1.1 in the easy direction; this is left as an exercise for the reader.

Delta-Matroids

Theorem 1.1 can be viewed as an excluded minor characterization for a class of delta-matroids. Let $\mathcal{F}$ be a collection of subsets of V. If $\mathcal{F}$ satisfies the symmetric exchange axiom (defined below) then $M = (V, \mathcal{F})$ is a *delta-matroid* (see Bouchet [1]).

(SEA) For $X, Y \in \mathcal{F}$ and $x \in X \Delta Y$ there exists $y \in X \Delta Y$ such that $X \Delta \{x, y\} \in \mathcal{F}$.

Let $M = (V, \mathcal{F})$ be a delta-matroid. It is easy to verify that, for any $S \subseteq V$, $(V, \mathcal{F} \Delta S)$ is also a delta-matroid, where $\mathcal{F} \Delta S = \{F \Delta S : F \in \mathcal{F}\}$; this operation is referred to as *twisting*. Also, $(V \backslash S, \{F \subseteq V \backslash S : F \in \mathcal{F}\})$ is a delta-matroid; we refer to this operation as *deletion*. Any delta-matroid that comes from M by twisting and/or deletion is referred to as a *minor* of M.

THEOREM 2.2 (Bouchet [3]). *Let A be a symmetric V by V matrix, and define $\mathcal{F}_A = \{S \subseteq V \colon A[S]$ is nonsingular$\}$. Then $M(A) = (V, \mathcal{F}_A)$ is a delta-matroid.*

Proof. Suppose $X, Y \in \mathcal{F}_A$ and $x \in X \Delta Y$ such that for all $y \in X \Delta Y$, $X \Delta \{x, y\} \notin \mathcal{F}_A$. Denote by $A' = (a_{ij})$ the matrix $A * X$. By Theorem 2.1, $A'[S]$ is nonsingular if and only if $S \Delta X \in \mathcal{F}_A$. By assumption $X \subseteq \{x\} \notin \mathcal{F}_A$, so $a_{xx} = 0$. However, $A'[X \Delta Y]$ is nonsingular, so there exists $y \in X \Delta Y$ such that $a_{xy} \neq 0$. Then, since $a_{xx} = 0$, $A'[\{x, y\}]$ is nonsingular. Therefore, $X \Delta \{x, y\} \in \mathcal{F}_A$, which is a contradiction. ∎

Bouchet proved that Theorem 2.2 also holds for skew-symmetric matrices. Delta-matroids arising from symmetric and skew-symmetric matrices are called *representable* (see [3]). A delta-matroid that can be represented by a symmetric PU-matrix is called *equable*. Deletion and twisting (by feasible sets) are both natural operations for representable delta-matroids. For $X \subseteq V$, the delta-matroid obtained by deleting X is $M(A[V \backslash X])$, and, for $X \in \mathcal{F}_A$, the delta-matroid obtained by twisting X is $M(A * X)$.

Let M be a binary delta-matroid (that is, a delta-matroid representable over $GF(2)$). Theorem 1.1 implies that M is representable by a symmetric PU-matrix if and only if M does not contain a minor isomorphic to $M(B_i)$, for $i = 1, ..., 5$. Bouchet and Duchamp [6] characterized the binary delta-matroids by excluded minors. Therefore we have an excluded minor characterization for the class of equable delta-matroids.

The following theorem shows that equable delta-matroids form a fundamental class of representable delta-matroids. (A referee noticed a gap in the original direct proof of the theorem and indicated how it could be fixed. However for brevity, we shall derive the theorem as a consequence of Theorem 1.1.)

THEOREM 2.3. *Let $M = (V, \mathcal{F})$ be a delta-matroid. The following are equivalent:*

(i) *M is equable,*

(ii) *M can be represented over every field by a symmetric matrix, and*

(iii) *M can be represented over both $GF(2)$ and $GF(3)$ by a symmetric matrix.*

Proof. That (i) implies (ii), and (ii) implies (iii) is easy. So it suffices to prove that (iii) implies (i). We shall prove the contrapositive.

Let M be a binary delta-matroid, and suppose that M is not equable. Then, by Theorem 1.1, M contains a minor that is isomorphic to one of the binary delta-matroids $M(B_1), ..., M(B_5)$. It is left to the reader to check that none of $M(B_1)$, ..., $M(B_5)$ is representable over $GF(3)$ by a symmetric matrix. Hence M cannot be represented over $GF(3)$ by a symmetric matrix. ∎

Support Graphs

The techniques used in the proof of Theorem 1.1 are mainly graphical. In this section we set up the notation. Let $A=(a_{ij})$ be a V by V symmetric matrix, we call V the *vertex set* of A. If $a_{vv}\neq 0$ then we call the vertex v a *loop-vertex* (otherwise v is a *nonloop-vertex*). We denote the set of loop-vertices by V_A^1. We now define a simple, undirected graph $G(A)=(V, E(A))$ such that $E(A)=\{vw: v\neq w, a_{vw}\neq 0\}$. $G(A)$ is called the *support graph* of A. Note that if A is a (0, 1)-matrix then A is uniquely defined by $G(A)$ and V_A^1. The support graphs of B_1, ..., B_5 are depicted in Fig. 2 (we have depicted the loop-vertices in bold).

Let $G=(V, E)$ be a graph. If $X\subseteq V$ then the graph *induced* by X, denoted $G[X]$, is the graph obtained by deleting the vertices in $V\backslash X$ from G. We denote by $N_G(X)$ the neighbour set of X, that is, the set of vertices in $V\backslash X$ that are adjacent to some vertex in X. For a vertex v, we denote $N_G(\{v\})$ by $N_G(v)$ and we denote $G[V\backslash\{v\}]$ by $G-v$. Similarly, for the symmetric matrix A, we denote $A[V\backslash\{v\}]$ by $A-v$. For a graph G' we denote by $V_{G'}$ and $E_{G'}$ its vertex set and edge set.

Let X be a subset of the vertices of A, and let A' be the matrix obtained by multiplying the rows and columns corresponding to vertices in X by -1. A' is symmetric, and A' is PU if and only if A is PU; furthermore, the set $\{uv: a_{uv}\neq a'_{uv}\}$ forms a cut of $G(A)$. We say that A and A' are equivalent under *cut-switching*. We refer to $-A$ as the *negation* of A. Two matrices A and B are said to be *equivalent under switching* if A is equivalent under cut-switching to either A or the negation of A.

Beta-Balancedness

Let G be a graph. A *signing* of G is an assignment of ± 1 to the edges of G. Suppose that, for every chordless circuit C of G, we assign a $\{0, 1\}$ value β_C to C. A *β-balanced signing* of G is a signing with the property

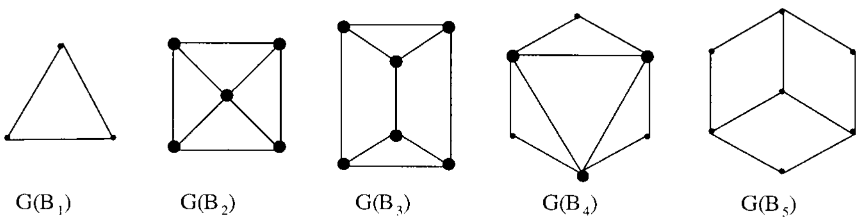

FIG. 2. Support graphs.

that. for every chordless circuit C, the number of edges of C signed $+1$ is equivalent to β_C modulo 2.

We now define two interesting classes of graphs. A *three-path configuration* is a graph of the form described in Fig. 3, where P_i is an induced path of length $|P_i|$, $i = 1, 2, 3$. The second class of graphs consists of the partial wheels; a graph G is a *partial wheel* with *hub* v if v is a vertex of degree at least 3 in G, and $G - v$ is a circuit. The following remarkable result is due to Truemper [10].

THEOREM 2.4. *Let G be a graph with $\{0, 1\}$ value β_C assigned to every induced circuit C of G. If G has no β-balanced signing then G contains an induced subgraph that is either a partial wheel or a three-path configuration, and which has no β-balanced signing.*

Elementary Pivoting

The following theorem about principal pivoting is implied by the quotient formula for the Schur complement (see Cottle *et al.* [8, p. 76]).

THEOREM 2.5. *Let $A[X]$ be a nonsingular principal submatrix of a square matrix A, and let $A * X[Y]$ be a nonsingular principal submatrix of $A * X$. Then $(A * X) * Y$ and $A * (X \Delta Y)$ are equivalent up to cut-switching.*

Let A be a symmetric matrix. Suppose that $A[X]$ is a nonsingular principal submatrix of A and that there exists $X' \subseteq X$ such that $A[X']$ is nonsingular. Then, by Theorem 2.5, $A * X$ and $A * X' * (X \backslash X')$ are equivalent up to cut-switching. We call $A * X$ an *elementary pivot* if there exists no proper subset X' of X such that $A[X']$ is nonsingular. Trivially, for each $v \in V_A^1$, $A * \{v\}$ is an elementary pivot. Define $V_A^2 = \{vw \in E(A) : v, w \notin V_A^1\}$. For each $vw \in V_A^2$, $A * \{v, w\}$ is also an elementary pivot. Furthermore, these are the only elementary pivots. We denote by $A * v$ and $A * vw$ the elementary pivots $A * \{v\}$ and $A * \{v, w\}$ respectively.

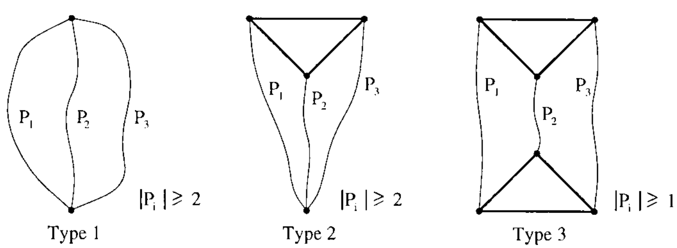

FIG. 3. Three-path configurations.

Let $A=(a_{ij})$ be a V by V symmetric (0, 1)-matrix. For a loop-vertex v of A, we have

$$A\times v=\left(\begin{array}{c|c}1 & \chi_v^T\\ \hline \chi_v & A[V-v]-\chi_v\chi_v^T\end{array}\right),$$

where χ_v is the submatrix of A indexed by rows $V-v$ and column v. We now describe the graphical effect of an elementary binary pivot. Let v be a vertex of a graph G. We define a graph $G\times v$ by replacing the induced subgraph $G[N_G(v)]$ by its complement; that is, $E(G)\,\Delta E(G\times V)=\{uw\colon u, w\in N_G(v)\}$. This operation is called *local complementation.* The following proposition is immediate from the definitions.

PROPOSITION 2.6. *If v is a loop-vertex of a symmetric* (0, 1)*-matrix A, then $G(A\times v)=G(A)\times v$ and $V^1_{A\times V}=V^1_A\,\Delta N_{G(A)}(v)$.*

Let $uw\in V^2_A$, and χ_i be the submatrix of A indexed by rows $V-u-w$ and column i. Thus

$$A=\left(\begin{array}{c|c|c}0 & 1 & \chi_u^T\\ \hline 1 & 0 & \chi_w^T\\ \hline \chi_u & \chi_w & A[V-u-w]\end{array}\right)$$

and

$$A\times uw=\left(\begin{array}{c|c|c}0 & 1 & \chi_w^T\\ \hline 1 & 0 & \chi_u^T\\ \hline \chi_w & \chi_u & A[V-u-w]-(\chi_w\chi_u^T+\chi_u\chi_w^T)\end{array}\right)$$

where the first and second rows are indexed by u and w. Graphically explaining the binary pivot in this case is more awkward. For a pair of disjoint subsets S, S' of V we define $[S, S']=\{ss'\colon s\in S, s'\in S'\}$. Let uw be an edge of a graph G. We define sets $S_u=(N_G(U)-w)\backslash N_G(w)$, $S_w=(N_G(w)-u)\backslash N_G(u)$, and $S_{uw}=N_G(u)\cap N_G(w)$. Now define an intermediate graph G' such that

$$E(G)\,\Delta E(G')=[S_u, S_w]\cup[S_u, S_{uw}]\cup[S_w, S_{uw}].$$

$G\times uw$ is obtained from G' by switching the vertex labels u and w. (Curiously, $G\times uw=G\times u\times w\times u$.) The following proposition follows from these definitions.

PROPOSITION 2.7. *Let A be a symmetric* $(0,1)$*-matrix. Then, for* $uw \in V_A^2$, $G(A \times uw) = G(A) \times uw$ *and* $V_{A\times uw}^1 = V_A^1$.

3. LOOP-BALANCED SIGNINGS

In this section we show that, to find a PU-signing of a matrix, we can sign the diagonal without knowing the signs of the nondiagonal entries. Let A be a symmetric $(0,1)$-matrix. For a path P of $G(A)$ we denote by $\kappa_A(P)$ the number of nonloop-vertices of P. A signing $A' = (a'_{ij})$ of A is called *loop-balanced* if, for every pair of loop-vertices v, w and every chordless (v, w)-path P, $a'_{vv} = (-1)^{\kappa_A(P)} a'_{ww}$. If $G(A)$ is connected then any two loop-balanced signings of A sign the loop-vertices equivalently under negation.

LEMMA 3.1. *Let A be a symmetric* $(0, \pm 1)$*-matrix such that $G(A)$ is a path. A is PU if and only if A is loop-balanced.*

Proof. If A has a zero diagonal, then, by an elementary determinant calculation, A is PU. Let v be a loop-vertex of A. If $A * v$ is not a $(0, \pm 1)$-matrix then, A is neither loop-balanced nor PU. If $A * v$ is a $(0, \pm 1)$-matrix, then $G(A * v) - v$ is a path; furthermore $A * v - v$ is loop-balanced if and only if A is loop-balanced. Hence the result follows inductively. ∎

The following lemma is an immediate consequence of Lemma 3.1.

LEMMA 3.2. *Let A be a symmetric* $(0, 1)$*-matrix. Then every PU-signing of A is loop-balanced.*

LEMMA 3.3. *Let A be a symmetric* $(0, 1)$*-matrix. If A has no loop-balanced signing then A reduces to B_1.*

Proof. Suppose A has no loop-balanced signing. We begin by proving the result in the special case that $G(A)$ is a circuit.

CLAIM. *If $G(A)$ is a circuit then A can be reduced to B_1.*

Let $G(A)$ be a circuit. Then A has no loop-balanced signing if and only if the following conditions are satisfied:

(i) A has an odd number of nonloop-vertices, and
(ii) there exist two loop-vertices that are not adjacent in $G(A)$.

We prove the result by induction on the size of A. By (ii), if A has size 3 then A has a loop-balanced signing. Suppose that A has size 4. By (i) and (ii), A has exactly three loop-vertices; let v be a loop-vertex whose neighbours in $G(A)$ are both loop-vertices. Then $(A \times v) - v$ is isomorphic to B_1.

Now suppose that A has size at least 5. By (ii), there exist two loop-vertices that are not adjacent in $G(A)$, and, by (i), A has at least one nonloop-vertex. Then, since A has size at least 5, there exist vertices v, v', w such that v, w are loop-vertices that are not adjacent in $G(A)$, and v' is a nonloop-vertex that is adjacent in $G(A)$ to v but not w. Note that $G(A\times v)-v$ is a circuit, and $A\times v-v$ has an odd number of nonloop-vertices. Furthermore, v', w are loop-vertices of $A\times v$ that are not adjacent in $G(A\times v)-v$; hence $(A\times v)-v$ has no loop-balanced signing. Then, by induction, $(A\times v)-v$ reduces to B_1, so A reduces to B_1, which proves the claim.

We now suppose that there exist loop-vertices v, w and a pair of chordless (v, w)-paths, $P_1=v, x_1, ..., x_a, w$ and $P_2=v, y_1, ..., y_b, w$ of $G(A)$ such that $\kappa_A(P_1)+\kappa_A(P_2)$ is odd. Furthermore, we suppose that the paths P_1 and P_2 are chosen so that $|V(P_1)\cup V(P_2)|$ is as small as possible.

Note that in $G(A\times v), P_1$ and P_2 are chordless (v, w)-paths, and $\kappa_{a\times v}(P_1)+\kappa_{A\times v}(P_2)$ is odd. Hence $A\times v$ is not loop-balanceable. Similarly, $A\times w$ is not loop-balanceable.

Suppose that $x_1=y_1$ we may assume, in this case, that x_1 is a loop vertex, for otherwise we can pivot on v. Now define $P'_1=x_1, ..., x_a, w$ and $P'_2=y_1, ..., y_b, w$; P'_1 and P'_2 are chordless (x_1, w)-paths such that $\kappa_A(P'_1)+\kappa_A(P'_2)$ is odd, and $|V_{P'_1}\cup V_{P'_2}|<|V_{P_1}\cup V_{P_2}|$, which is a contradiction. Hence, we may assume that $x_1\neq y_1$; similarly we may assume that $x_a\neq y_b$. We may also assume that x_1y_1 is not an edge, since otherwise pivoting on v would remove it. Similarly, we may assume that x_ay_b is not an edge.

If $v, x_1, x_2, ..., x_a, w, y_b, y_{b-1}, ..., y_1$ is a chordless circuit then, by the claim, we can reduce A to B_1. Hence we may assume that there exists an edge x_iy_j in $G(A)$. Let i be minimum such that x_i is adjacent to some y_j, and let j be maximum such that y_j is adjacent to x_i. Let P be the path $v, x_1, ..., x_i, y_j, ..., y_b, w$; note that P is chordless. Now let P' be one of P_1, P_2 such that $\kappa_A(P')\not\equiv\kappa_A(P)$ modulo 2. However, $|V(P)\cup V(P')|<|V(P_1)\cup V(P_2)|$. Hence we have a contradiction to the choice of P_1, P_2.

Therefore, for every pair of loop-vertices v, w, and every pair of chordless (v, w)-paths P_1, P_2, we have $\kappa_A(P_1)\equiv\kappa_A(P_2)$ modulo 2; denote by $\kappa(v, w)$ the value $\kappa_A(P_1)$. We may assume that $G(A)$ is connected, so $\kappa(v, w)$ is well defined modulo 2, for every pair v, w of loop-vertices. Let x_1 be a loop-vertex of A. Define a signing $A'=(a_{ij})$ of A such that $a'_{x_1x_1}=+1$ and, for every other loop-vertex v of A, $a'_{vv}=(-1)^{\kappa(v, x_1)}$. Since A has no loop-balanced signing, A' is not loop-balanced, so there exist loop-vertices x_2, x_3 such that $a'_{x_2x_2}\neq(-1)^{\kappa(x_2, x_3)}a'_{x_3x_3}$. Therefore $\kappa(x_2, x_3)+\kappa(x_1, x_3)+\kappa(x_1, x_2)$ is odd.

Let $X\subseteq V$ be minimal such that X contains x_1, x_2, x_3 and $G(A[X])$ is connected. For each i, j, let P_{ij} be a chordless (x_i, x_j)-path in $G(A[X])$. The union of any two of the paths P_{12}, P_{23}, P_{13} yields a connected graph containing the vertices x_1, x_2, x_3. Therefore, by the minimality of X, each

$x \in X$, is contained in at least two of the paths P_{12}, P_{23}, P_{13}. However, since $\kappa_A(P_{12}) + \kappa_A(P_{13}) + \kappa_A(P_{23})$ is odd, there must exist a nonloop-vertex x that is contained in all three paths P_{12}, P_{13}, P_{23}. Then, since the paths P_{ij} are chordless, for $i = 1, 2, 3$, there is a unique (x, x_i)-path P_i in $G(A[X])$, and every edge of $G(A[X])$ is on one of these paths.

We claim that $A[X]$ reduces to B_1. We may assume that for $i = 1, 2, 3$, x_i is the only loop-vertex of $A[X]$ on path P_i, since, otherwise we replace x_i by the closest loop-vertex to x on P_i, and redefine X accordingly. Furthermore, we may assume that P_i has length 1, since otherwise we shorten P_i by pivoting on x_i, and then deleting x_i from X. Then $A[X] \times x_1 \times x - x$ is isomorphic to B_1. ∎

4. BALANCEABLE MATRICES

We begin this section by proving some basic facts about circuits.

LEMMA 4.1. *Let A be a loop-balanced $(0, \pm 1)$-matrix such that $G(A)$ is a circuit, and let $X \subseteq V$ such that $|X| \leqslant |V| - 3$. If $A[X]$ is nonsingular then $G(A * X)[V \backslash X]$ is a circuit, and $A * X[V \backslash X]$ is PU if and only if A is PU.*

Proof. By Theorem 2.1 and Lemma 3.1, $A * X[V \backslash X]$ is PU if and only if A is PU. To see that $G(A * X)[V \backslash X]$ is a circuit, it suffices to check the elementary pivots, for which the result is obvious. ∎

LEMMA 4.2. *Let A be a $(0, 1)$-matrix such that $G(A)$ is a circuit. If A has no PU-signing then A reduces to B_1.*

Proof. Suppose that A has no PU-signing. By Lemma 3.3, we may assume that A has a loop-balanced signing. By Lemma 4.1, we can reduce A to either a matrix of size 3, or a matrix of size 4 that has no loop-vertices. If $G(A)$ is a circuit of length 3, and $A \neq B_1$ then there exists a loop-vertex v of A. Thus $G(A \times v)$ is a path, so by Lemma 3.1, A has a PU-signing. If $G(A)$ is a circuit of length 4, and A has no loop-vertices then, for an edge vw of $G(A)$, $G(A \times vw)$ is a path, so A has a PU-signing. ∎

LEMMA 4.3. *Let A be a $(0, 1)$-matrix such that $G(A)$ is a circuit. Any two PU-signings of A are equivalent under switching.*

Proof. By Lemma 4.1, it suffices to check the result for circuits of length 3 or 4; this is left to the reader. ∎

We call a symmetric $(0, \pm 1)$-matrix A *balanced* if A is loop-balanced and, for every induced circuit C of $G(A)$, $A[V(C)]$ is PU. A symmetric $(0, 1)$-matrix A is called *balanceable* (otherwise it is *nonbalanceable*) if it has a balanced signing. The following lemma is a generalization of a theorem of Camion [7] for totally unimodular matrices.

LEMMA 4.4. *Let A be a symmetric $(0, 1)$-matrix, such that $G(A)$ is connected. Any two balanced signings of A are equivalent under switching. In particular, any two PU-signings of A are equivalent under switching.*

Proof. Let $A_1 = (a_{ij}^1)$ and $A_2 = (a_{ij}^2)$ be balanced signings of A. The diagonals of A_1 and A_2 are equivalent up to reversing, so we may assume that they are the same. Define $S = \{ij: a_{ij}^1 \neq a_{ij}^2\}$. By Lemma 4.3, for each chordless circuit C of G, $|E(C) \cap S|$ is even. Hence for each circuit C of G, $|E(C) \cap S|$ is even. Therefore the edge set S is a cut in $G(A)$, so A_1 and A_2 are equivalent under cut-switching. ▮

We define an *obstruction* to be a symmetric $(0, 1)$-matrix, that does not reduce to B_1, that does not admit a PU-signing, and that does not reduce to any smaller matrix with these properties.

LEMMA 4.5. *Let A be a balanceable obstruction, and let $X \subseteq V$ such that $|X| \leqslant |V| - 3$ and $A[X]$ is nonsingular. Then $G(A \times X)[V \backslash X]$ is a circuit.*

Proof. Let A' be a balanced signing of A. If $Y \subseteq V$ and $A'[Y]$ is not unimodular then, by Lemma 4.4, $A[Y]$ has no PU-signing. Therefore, since A is an obstruction, the only principal submatrix of A' that is not unimodular is A' itself. By Theorem 2.1, the only principal submatrix of $A' * X$ that is not unimodular is $A' * X[V \backslash X]$. If $A' * X$ is balanced then $A \times X[V \backslash X]$ has no PU-signing, contradicting that A is an obstruction. Therefore $A' * X$ is not balanced; and, since $A' * X[V \backslash X]$ is the only non-unimodular submatrix of $A' * X$, $G(A' * X)[V \backslash X]$ must be a circuit. ▮

The following proposition removes some trivial cases; the proof is left as an exercise. Note that if A is an obstruction, then $G(A)$ is connected, and $G(A)$ is neither a path nor a circuit. There are, up to isomorphism, just four such graphs with at most four vertices.

PROPOSITION 4.6. *Every obstruction has size at least* 5.

LEMMA 4.7. *If A is an obstruction, then A is equivalent under binary pivoting to a non-balanceable obstruction.*

Proof. Suppose, by way of contradiction, that A is an obstruction and every matrix equivalent to A under pivoting is balanceable.

CLAIM. *If $X \subseteq V$ such that $|X| \leqslant |V| - 3$, and $A[X]$ is nonsingular, then $G(A)[V \backslash X]$ and $G(A \times X)[V \backslash X]$ are both circuits.*

Since $A[X]$ and $A \times X[X]$ are nonsingular, and A and $A \times X$ are balanceable, the claim follows by Lemma 4.5.

Suppose that A has a loop-vertex x. Let y be a neighbour of x in $G(A)$. We may assume that y is a not a loop-vertex, since otherwise we could make y a nonloop-vertex by pivoting on x. Both $A[\{x\}]$ and $A[\{x, y\}]$ are nonsingular. Then, by the claim, $G(A) - x$ and $G(A) - x - y$ are both circuits, which is clearly impossible. Hence A has no loop-vertices.

Since A has no loop-vertices and A does not reduce to B_1, $G(A)$ is bipartite. By the claim, for every edge vw of $G(A)$, $G(A) - v - w$ is a circuit. Let v_1, v_2, v_3, v_4 be consecutive vertices in any such circuit. We may assume that $v_1 v_4$ is not an edge, since otherwise we can remove the edge by pivoting on $v_2 v_3$. Since $G(A) - v_2 - v_3$ is a circuit and $v_1 v_4$ is not an edge, v_1 has degree 3 in $G(A)$. However, v_1 is adjacent to neither v_3 nor v_4, which contradicts that $G(A) - v_3 - v_4$ is a circuit. ∎

5. NONBALANCEABLE MATRICES

The problem has now simplified to finding the nonbalanceable obstructions. This task is made easy by the following lemma.

LEMMA 5.1. *Let A be a nonbalanceable obstruction. Then $G(A)$ is either a three-path configuration or a partial wheel.*

Proof. Recall that B_1 is not considered an obstruction. Then, by Lemma 3.3, A has a loop-balanced signing, say $A' = (a'_{ij})$. For each induced circuit C of $G(A)$, let $H_C = A[V(C)]$. Then, by Lemma 4.2, H_C has a PU-signing, say $H'_C = (h'^C_{ij})$. We may assume that for every loop-vertex v of H_C, $h'^C_{vv} = a'_{vv}$ (otherwise we negate H'_C). We now define β_C to be 0 (respectively 1) if the number of edges vw of C with $h'^C_{vw} = +1$ is even (respectively odd). By Lemma 4.3, $A'[V(C)]$ is PU if and only if it is equivalent under cut-switching to H'_C, that is, the number of edges vw of C with $a'_{vw} = +1$ is equivalent to β_C modulo 2. Hence A is balanceable if and only if $G(A)$ has a β-balanced signing. The result then follows by Theorem 2.4. ∎

LEMMA 5.2. *Let A be a nonbalanceable obstruction, and let $X \subseteq V$ such that $|X| \leqslant |V| - 3$, $A[X]$ is nonsingular, and $G(A)[V \backslash X]$ is not a circuit. Then $A \times X$ is not balanceable. Furthermore, if $X = \{v\}$, then $N_{G(A)}(v)$ is not a stable set of $G(A)$.*

Proof. If $A \times X$ is balanceable then, by Lemma 4.5, $G(A)[V \backslash X] = G((A \times X) \times X)[V \backslash X]$ is a circuit, a contradiction. Therefore, $A \times X$ is a nonbalanceable obstruction. Now suppose that $X = \{v\}$, and that $N_{G(A)}(v)$ is a stable set of $G(A)$. Then $N_{G(A)}(v)$ induces a clique of $G(A \times v)$. However, by Lemma 5.1, $G(A \times v)$ is a three-path configuration or a partial wheel, so it must be the case that $G(A \times v)$ is the complete graph on 4 vertices, contradicting Proposition 4.6. ∎

LEMMA 5.3. *Let A be a nonbalanceable obstruction such that $G(A)$ is a three-path configuration. Then $G(A)$ is isomorphic to $G(B_3)$.*

Proof. First suppose that $G(A)$ is a three-path configuration of Type 1 or Type 2. Let w be a vertex of degree 3 in $G(A)$ such that $N_{G(A)}(w)$ is a stable set. By Lemma 5.2, w is not a loop-vertex. If all three vertices adjacent to w in $G(A)$ are loop-vertices then A is not loop-balanceable, which, by Lemma 3.3, is a contradiction. Therefore there exists a nonloop-vertex v adjacent to w in $G(A)$. This is depicted in Fig. 4. $G(A) - v - w$ is not a circuit; so, by Lemma 5.2, $A \times vw$ is nonbalanceable. Therefore, by Lemma 5.1, $G(A \times vw)$ is a three-path configuration or a partial wheel. Note that, in $G(A \times vw)$, either w is adjacent to a vertex of degree at least 4, or v is adjacent to a vertex of degree 1. This is a contradiction, since a three-path configuration or a partial wheel can have neither a vertex of degree 1 nor a vertex of degree 2 that is adjacent to a vertex of degree at least 4.

Now, suppose that $G(A)$ is a three-path configuration of Type 3, and that $G(A)$ is not isomorphic to $G(B_3)$, one of the paths, say P_3, has length at least 2. Let v be an end vertex of P_3, and let w be the vertex of P_3 that is adjacent to v, as depicted in Fig. 5. By Lemma 5.2, w is a nonloop-vertex. $G(A) - v$ is not a circuit, so, by Lemma 4.5, if v is a loop-vertex then $A \times v$ is nonbalanceable. However, $G(A \times v)$ is neither a three-path configuration nor a partial wheel, which is a contradiction. Therefore we may assume that v is a nonloop-vertex. Now $G(A) - v - w$ is not a circuit; so, by Lemma 5.2, $A \times vw$ is nonbalanceable. However, $G(A \times vw)$ is neither a three-path configuration nor a partial wheel, which is a contradiction. ∎

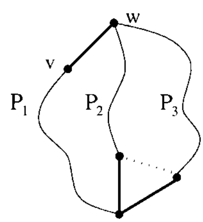

FIG. 4. Three path configuration, Type 1 or Type 2.

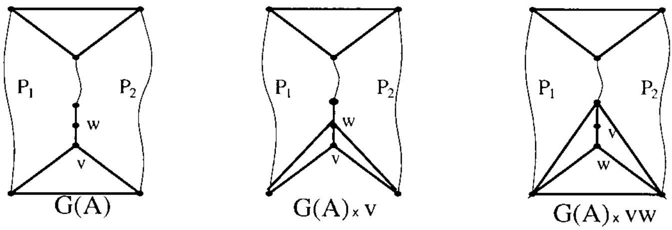

FIG. 5. Three path configuration, Type 3

LEMMA 5.4. *Let A be a nonbalanceable obstruction such that $G(A)$ is a partial wheel, and let C be an induced circuit of $G(A)$. Then, for every edge vw of $G(A)$ that is not an edge of C, $|N_{G(A)}(\{v, w\}) \cap V(C)| \geqslant 2$; in particular $G(A)$ contains no pair of adjacent vertices of degree* 2.

Proof. Suppose there exists an edge vw of $G(A)$ such that $N_{G(A)}(\{v, w\}) \cap V(C)| \leqslant 1$. Let x be the hub of the partial wheel; C must contain the vertex x and vw must be an edge of $G(A) - x$. Suppose that v and w are adjacent vertices of degree 2. By Lemma 5.2, neither v not w are loop-vertices. Now $G(A) - v - w$ is not a circuit, so, by Lemma 5.2, $A \times vw$ is not balanceable. However, $G(A \times vw)$ contains an edge $v'w'$ such that $G(A \times vw) - v' - w'$ is not connected, so $G(A \times vw)$ is neither a partial wheel nor a three-path configuration, contradicting Lemma 5.1. Thus, we may assume that at least one of v and w is adjacent to x. Then neither v nor w may be adjacent to any vertex of C other than x; this is depicted in Fig. 6. In this case A must have size at least 7.

Suppose that v is a loop-vertex. Then, by Lemma 5.2, $G(A \times v)$ is a three-path configuration or a partial wheel. However, $G(A \times v)$ has a pair of vertex disjoint circuits, so it is not a partial wheel. Therefore, $G(A \times v)$ is a three-path configuration, so, by Lemma 5.3, $G(A \times v)$ is isomorphic to $G(B_4)$, contradicting that A has size at least 7. Hence, we may assume that v (and, similarly, w) is not a loop-vertex.

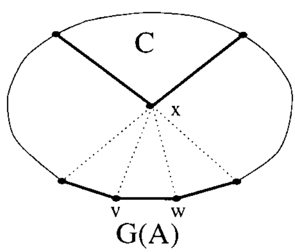

FIG. 6. Partial wheel.

By Lemma 5.2, $G(A \times vw)$ is a three-path configuration or a partial wheel. However, $G(A \times vw)$ has a pair of vertex disjoint circuits, so it is not a partial wheel. Therefore, $G(A \times vw)$ is a three-path configuration, so, by Lemma 5.3, $G(A \times vw)$ is isomorphic to $G(B_4)$, contradicting that A has size at least 7. ∎

The proof is now reduced to case analysis. We hide much of it in the following lemma.

LEMMA 5.5. *Let A be a nonbalanceable obstruction such that $G(A)$ is isomorphic to one of the graphs depicted in Fig. 7. Then A reduces to B_2, B_3 or B_4.*

Before beginning the case analysis for Lemma 5.5, we use it to prove the main result.

Proof of Theorem 1.1. Let A be an obstruction. We are required to prove that A is equivalent under binary pivoting to one of $B_2, ..., B_5$. By Lemma 4.7, we may assume that A is nonbalanceable. Then, by Lemma 5.1. $G(A)$ is either a three-path configuration, or a partial wheel.

Suppose that $G(A)$ is a three-path configuration. Then, by Lemma 5.3, $G(A)$ isomorphic to $G(B_3)$. Let x_1, x_2, x_3 be vertices that induce a triangle of $G(A)$; at least one x_i, say x_1, must be a loop-vertex (otherwise A reduces to B_1). $G(A) - x_1$ is not a circuit, so $A \times x_1$ is nonbalanceable. However, $G(A \times x_1)$ is isomorphic to G_5 of Fig. 7, so, by Lemma 5.5, A is equivalent under binary pivoting to B_2, B_3, or B_4.

Now suppose that $G(A)$ is a partial wheel. By Lemmas 5.4 and 5.5 and Proposition 4.6, we may assume that A has size at least 7. Let C be a shortest circuit of $G(A)$. By Lemma 5.5, C has length 3 or 4. If $|V_{G(A)}| \geqslant |V_C| + 4$ then there exists an edge vw of G that is not an edge of C, such that $|N_{G(A)}(\{v, w\}) \cap V_C| \leqslant 1$ contradicting Lemma 5.4. Then C cannot have length 3, since otherwise A would have fewer than seven vertices. Hence C has length 4, and A has size exactly 7. $G(B_5)$ is the unique partial wheel, up to isomorphism, with seven vertices and no circuit of length 3. Therefore $G(A)$ is isomorphic to $G(B_5)$. Let x be the hub of $G(A)$. By Lemma 5.2, every vertex of A other than x is a nonloop-vertex. If x is also

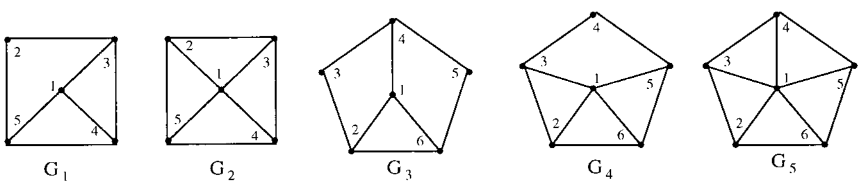

FIG. 7. Awkward cases.

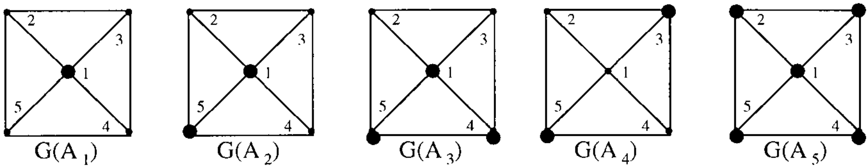

FIG. 8. Loop-vertices for G_2.

a nonloop-vertex, then A is equivalent to B_5; otherwise if x is a loop-vertex, then $(A \times x) - x$ is equivalent to B_4, a contradiction. ∎

Proof of Lemma 5.5. Suppose that $G(A)$ is isomorphic to G_2. Note that A must be loop-balanceable. There are, up to isomorphism, five choices for the loop-vertices of $A-1$, and each choice uniquely determines whether or not 1 is a loop-vertex. The possibilities are depicted in Fig. 8. $G(A_i \times 1 \times 2 \times 3)$ is a path for $i = 1, 2, 3$, so these matrices are not obstructions. $G(A_4) - 1 - 3$ is not a circuit, but $G(A_4 \times \{1, 3\})$ is neither a partial wheel nor a three-path configuration, so, by Lemma 5.2, A_4 is not an obstruction. A_5 is isomorphic to B_2.

Suppose that $G(A)$ is isomorphic to G_1. By Lemma 5.2, 2 is not a loop-vertex of A. We may assume that neither 3 nor 5 are loop-vertices of A, since $G_1 \times 3$ and $G_1 \times 5$ are both isomorphic to G_2. Therefore one of 1,4 must be a loop vertex; we assume by symmetry that 1 is a loop-vertex. However, $G(A \times 1 \times 5 \times 2)$ is a path, so A is not an obstruction.

Suppose that $G(A)$ is isomorphic to G_4. By Lemma 5.2, 3, 4 and 5 are all not loop-vertices. However, $G_4 - 1$ is an odd circuit, so either 2 or 6 must be a loop-vertex; we assume by symmetry that 2 is a loop-vertex. $G(A \times 2)$ and $G(A \times 2 \times 45)$ are depicted in Fig. 9. (The vertices indicated by squares may or may not be loop vertices.) By Lemma 5.2, 1 is a nonloop-vertex in $A \times 2$, and 6 is a nonloop-vertex of $A \times 2 \times 45$; hence, 1 and 6 are both loop vertices of A. Thus, the loop-vertices of A are 1, 2 and 6, so, $A \times 1$ is isomorphic to B_4.

Suppose that $G(A)$ is isomorphic to G_3. By Lemma 5.2, 3, 4, and 5 are all not loop-vertices. However, $G_3 - 1$ is an odd circuit, so either 2 or 6

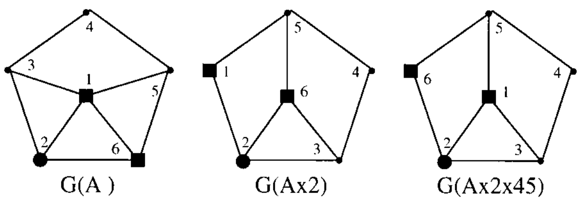

FIG. 9. Pivoting in G_4.

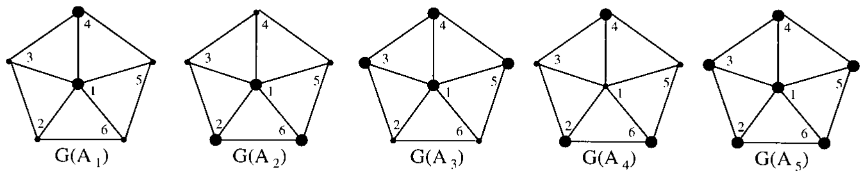

FIG. 10. Loop-vertices for G_5.

must be a loop-vertex; we assume by symmetry that 2 is a loop-vertex. However $G(A\times 2)$ is isomorphic to G_4, so A reduces to B_4.

Finally, suppose that $G(A)$ is isomorphic to G_5. There are, up to isomorphism, five choices for the loop-vertices of $A-1$ so that $A-1$ does not reduce to B_1. Each choice uniquely determines whether or not 1 is a loop-vertex; the possibilities are depicted in Fig. 10. $A_i\times 1-1$ reduces to B_1 for $i=1, 2, 3, 5$, so these matrices are not obstructions. $A_4\times 4$ is isomorphic to B_3. ∎

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REFERENCES

1. A. Bouchet, Greedy algorithm and symmetric matroids, *Math. Programming* **38** (1987), 147–159.
2. A. Bouchet, Unimodularity and circle graphs, *Discrete Math.* **66** (1987), 203–208.
3. A. Bouchet, Representability of Δ-matroids, *Colloq. Soc. Janos Bolyia* **52** (1988), 167–182.
4. A. Bouchet, A characterization of unimodular orientations of simple graphs, *J. Combin. Theory Ser. B* **56** (1992), 45–54.
5. A. Bouchet, W. H. Cunningham, and J. F. Geelen, Unimodularity of principal submatrices of skew-symmetric matrices, in preparation.
6. A. Bouchet and A. Duchamp, Representability of Δ-matroids over $GF(2)$, *Linear Algebra Appl.* **146** (1991), 67–78.
7. P. Camion, Caractérisation des matrices unimodulaires, *Cahiers Centre Études Rech. Opér.* **5** (1963), 181–190.
8. R. W. Cottle, J.-S. Pang, and R. E. Stone, "The Linear Complementarity Problem," Academic Press, San Diego, 1992.
9. A. M. H. Gerards, A short proof of Tutte's characterization of totally unimodular matrices, *Linear Algebra Appl.* **114/115** (1989), 207–212.
10. K. Truemper, Alpha-balanced graphs and matrices and $GF(3)$-representability of matroids, *J. Combin. Theory Ser. B* **32** (1982), 112–139.
11. W. T. Tutte, A homotopy theorem for matroids, I, II, *Trans. Amer. Math. Soc.* **88** (1958), 144–174.
12. W. T. Tutte, Lectures on matroids, *J. Res. Nat. Bur. Stand. Sect. B* **69** (1965), 1–47.