Transient stability and power flow model of the Unified Power Flow controller for various control strategies

Claudio A. Cañizares

University of Waterloo, Department of Electrical & Computer Engineering, Waterloo, ON, Canada, N2L 3G1, C.Canizares@ece.uwaterloo.ca

Edvina Uzunovic

New York Power Authority, White Plains, NY, USA, Edvina.Uzunovic@nypa.gov

John Reeve

University of Waterloo, Department of Electrical & Computer Engineering, Waterloo, ON, Canada, N2L 3G1

Abstract: This paper describes and validates transient stability and power flow model of a Unified Power Flow Controller (UPFC), and presents a detailed comparison of different controls strategies, proposing novel, efficient and simple controls for this controller. The proposed model accurately represents the behavior of the controller in quasi-steady state operating conditions, and hence is adequate for transient as well as steady state stability analyses of power systems. The model is validated with the help of the Electromagnetic Transient Program (EMTP), where a detailed model of the controller is implemented and then compared to the suggested stability model. A realistic 11-bus test system is used here to validate the proposed model and compare the different controls. The UPFC is simulated in this test system under different operating conditions using both the detailed and "reduced" models and diverse control strategies.

Keywords: FACTS, UPFC, EMTP, transient stability, steady state, power flow, modeling, controls, power oscillation damping.

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Biographical Notes: Claudio A. Cañizares received the Electrical Engineer diploma in April 1984 from the Escuela Politécnica Nacional (EPN), Quito-Ecuador, where he held different teaching and administrative positions from 1983 to 1993. His MS (1988) and PhD (1991) degrees in Electrical Engineering are from the University of Wisconsin-Madison. Dr. Cañizares is currently a Professor at the University of Waterloo, E&CE Department, and his research

activities are mostly concentrated in studying stability, modeling and computational issues in ac/dc/FACTS systems.

Edvina Uzunovic was born in Sarajevo, Bosnia-Herzegovina. She graduated from the University of Sarajevo in Electrical Engineering in 1990. After professional positions in Sarajevo, she joined the Department of Electrical \& Computer Engineering at the University of Waterloo as a graduate student in 1993, where she completed her M.A.Sc. degree with a research thesis in voltage stability of ac/dc transmission systems in 1995, and is currently a Ph.D. student. She is currently working at the New York Power Authority.

John Reeve received the B.Sc., M.Sc., Ph.D. and D.Sc. degrees from the University of Manchester (UMIST). After employment in the development of protective relays for English Electric, Stafford, between 1958 and 1961, he was a lecturer at UMIST until joining the University of Waterloo in 1967, where he is currently an Adjunct Professor in the Department of Electrical & Computer Engineering. He was a project manager at EPRI, 1980-81, and was with IREQ, 1989-1990. His research interests since 1961 have been HVDC transmission and high power electronics. He is the President of John Reeve Consultants Limited. Dr. Reeve was chair of the IEEE DC Transmission Subcommittee for 8 years, and is a member of several IEEE and CIGRE Committees on dc transmission and FACTS. He was awarded the IEEE Uno Lamm High Voltage Direct Current Award in 1996.

1 Introduction

In recent years, there has been growing interest in the use of Flexible AC Transmission Systems (FACTS) controllers in power transmission applications [1]. One FACTS controller in particular, the Unified Power Flow Controller (UPFC), is capable of concurrently or selectively controlling transmission line power flows, voltage magnitudes and phase angles in a power system [2, 3]. Hence, it is expected that its use and control applications will grow, particularly in new deregulated markets where simultaneous, independent and fast controls of active and reactive power flows are an asset. The UPFC controller brings major benefits in steady state operation of power systems as well as in emergency situations, where it will be possible to rapidly and effectively redirect power flows and/or damp power oscillations [4]. A ± 320 MVA, 138 kV UPFC has been recently commissioned for the American Electric Power [5, 6], and another project involving a ± 200 MVA, 345 kV UPFC is just under way. The latter is being referred to as a Convertible Static Compensator and is about to be installed by the New York Power Authority (NYPA) [7].

1.1 UPFC Modeling

UPFC models have been investigated by several authors [8]. In [9], for example, the UPFC model consists of a controllable voltage source added in series with the transmission line, plus two current sources added in shunt to balance the power flow through the controller. The UPFC model given in [10] is made up of two ideal

synchronous voltage sources connected in shunt and series to the transmission line. In [11], the external macro capabilities of a popular power system analysis software are used to model the UPFC using a coupled-source model, as series voltage source models are generally not available in commercial power system software packages. A model in [12] properly represents the dc part of the device; but the losses in the converter circuits are not included. All these papers lack an adequate validation of the proposed models, which are not compared to a detailed UPFC model under realistic study situations typically encountered in transient stability analysis.

The current paper addresses the outstanding UPFC modeling problems by proposing and validating a transient stability and power flow model of the UPFC based on the ideas presented in [13]. The model for the UPFC is developed using a power balance equation that couples the shunt and series ac/dc converters through its common dc link, as well as through their physical system connections, as initially proposed in [14]. The proposed controller model is then validated by comparing it to a detailed model that includes all switching devices as well as their corresponding snubbers, by means of realistic simulations of typical transient stability conditions carried out in the EMTP for a detailed 11-bus test system.

1.2 UPFC Controls

This paper also deals with the issues of adequate controls and applications of the UPFC, based on the many references available in the literature that discuss different studies and applications of the UPFC using a variety of tools, controls and models. Thus, [6] illustrates the operation of the UPFC under fault conditions using a TNA to demonstrate how a UPFC significantly influences the steady state and dynamic operation of a power system. The impact of the UPFC on voltage stability, tested on a multi-machine test system using an in-house developed program, is discussed in [15]. In [16], the effect of a UPFC on the transient stability margins of a power system is analyzed; the results in this case are obtained using a simple test system modeled in NETOMAC. SIMULINK is used in [17] to evaluate the effect of a UPFC control strategy to damp power oscillations. In [18], a decoupled PQ controller of active (P) and reactive (Q) power is proposed, whereas in [19], the authors propose a simpler P-Q controller, based on a decomposition of the series injected voltage of the UPFC, discussing the way the different controller limits should be handled within the proposed controls.

Based on these papers and results, the current paper investigates the UPFC capabilities in power oscillation damping mode using the detail model implemented in the EMTP, proposing simple and effective controls for both shunt and series converters.

The paper is structured as follows: In Section 2, the UPFC basic operating and control principles are briefly described; the basic issues related to the implementation of the UPFC models in the EMTP are also discussed here. The proposed transient stability and power flow model is presented and thoroughly justified in this section as well, presenting the equations and limit handling procedures needed to adequately represent the UPFC in both transient stability and power flow programs. Section 3 discusses various control strategies for both shunt and series converters of the UPFC. The results obtained from various simulations in a 11-bus test system for detailed EMTP and stability models under

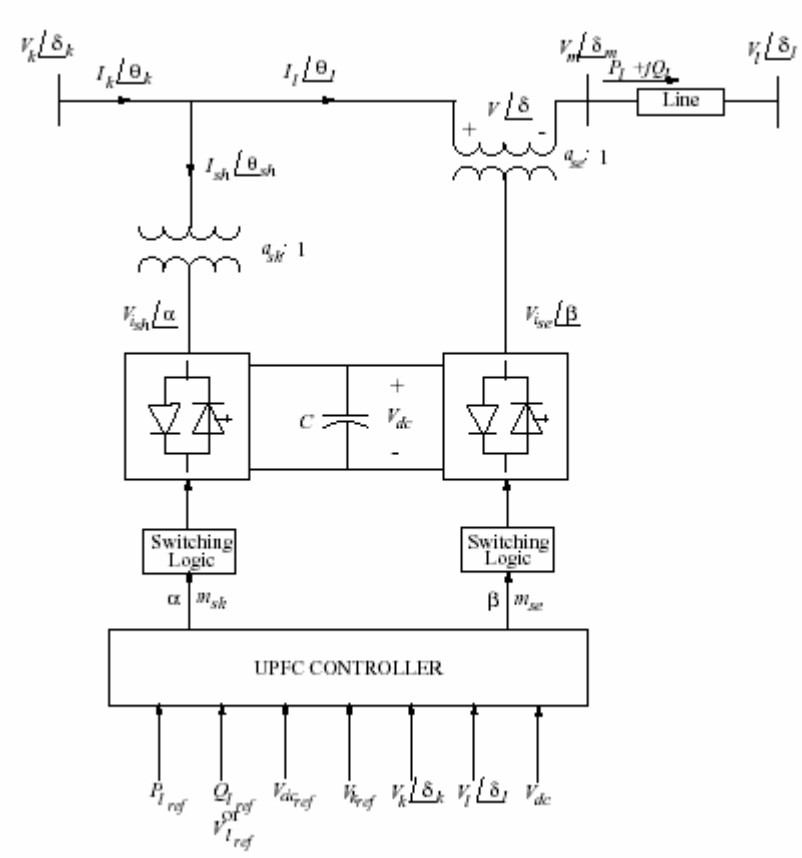
different control strategies are presented and compared in Section 4. Finally, Section 5 summarizes the main contributions of the paper and suggests future research directions.

2 UPFC Modeling

The basic structure and operation of the UPFC is well known and described in numerous technical publications. For this reason, the basic operation of a UPFC is only explained briefly here; the interested reader is referred to [20, 21] for more information on this subject.

The UPFC is made out of two voltage-source converters (VSC) with semiconductor devices having turn-off capability, sharing a common dc capacitor and connected to a power system through coupling transformers. The basic UPFC structure is depicted in Figure 1. This figure represents both pulse-width modulation (PWM) and phase control strategies.

Figure 1 UPFC functional model.



The main objective of the series converter is to produce an ac voltage of controllable magnitude and phase angle, and inject this voltage at fundamental frequency into the transmission line, exchanging real and reactive power at its ac terminals through the series connected transformer. The shunt converter provides the required real power at the dc terminals; thus, real power flows between the controller shunt and series ac terminals

through the common dc link. The reactive power is generated/absorbed independently by each converter and does not flow through the dc link [2, 3].

There are two basic control strategies that can be utilized to control the switching of the semiconductor switches in the converters, i.e., PWM and phase controls. GTO switches operate adequately at the "low" switching frequencies required in phase control, but present high losses at the "high" switching frequencies needed for PWM control. However, recent advances in high voltage IGBT technology have led to the development of the Integrated Gate Commutated Thyristor (IGCT), which is basically an optimum combination of thyristor and GTO technology at low cost, low complexity, and high efficiency [22]. It can handle higher switching frequencies with relatively low losses, allowing for the practical implementation of PWM control methodologies.

The phase control approach involves properly multi-connected phase-shifted converters with a common dc source and coupled through appropriate magnetic circuits. In an actual UPFC implementation, this technique is used to connect 4 multi-level converters operating in a 48-pulse structure to generate almost harmonic-free voltage output waveforms. The PWM technique, on the other hand, is based on fast switching of semiconductor switches to produce an output voltage waveform with low harmonic content, which depends on the number of notches per cycle. The advantage of this technique is that it allows independent and easy control of active and reactive power components, provided that the dc voltage is kept constant and sufficiently high.

2.1 Detailed EMTP Model

In this paper, the converter controllable switches are modeled using a general EMTP-TACS controllable switch model, while the corresponding diodes are modeled using the diode model provided in the EMTP [23]. These are all ideal switches; hence, to somewhat account for losses in the converter circuit and satisfy basic connection requirements in the EMTP a resistor between two switches is inserted.

The UPFC simulated here is made out of two VSCs with a Sinusoidal PWM (SPWM) controller. The modulation ratio that specifies the harmonic content in the output voltage waveform is kept at a moderate level of 15 to make the study realistic. The PWM reference signal is made of two sinusoidal waveforms, at fundamental frequency waveform and the second one at the third harmonic, so that the fundamental component of the converter output voltage is increased [24]. Even and triple harmonics are not present on the output voltage waveform, and 13th, 17th, 29th, 31st harmonics are reduced using passive filters placed on the secondary side of the transformers.

The UPFC shunt and series transformers are modeled as banks of three ideal single-phase two-winding transformers with no saturation. The transformer ratings are calculated according to the permissible maximum shunt current, maximum shunt voltage, maximum series (transmission line) current and maximum series inserted voltage, as shown in Section 4. Except for the maximum shunt voltage, which is defined by the kV rating of the power system, the other parameters are defined based on design and operating conditions [6].

2.2 Transient Stability Model

In balanced conditions, the converter output voltage waveform is basically a fundamental frequency sinusoid, given the presence of harmonic filters. Hence, the VSCs can be accurately represented as voltage sources operating at fundamental frequency for transient and steady state stability studies, where transient oscillations are in the order of 2-3 Hz under balanced operating conditions (quasi-steady-state operation). Consequently, the UPFC may be modeled as illustrated in Figure 2.

This model is based on a power balance technique, similar to the one proposed in [21] and used in [13] to develop a STATCOM model, i.e.,

$$P_{ac} = P_{dc} + P_{losses} \tag{1}$$

Thus, the three-phase instantaneous power flowing into the shunt converter from the ac bus, neglecting transformer losses and assuming fundamental frequency and balanced conditions, can be represented by

$$p_{sh} = 3\ V_k I_{sh} \cos(\delta_k - \theta_{sh}) \tag{2}$$

where $V_k\angle\delta_k$ is the rms phasor of the sinusoidal sending-end voltage v_k, and $I_{sh}\angle\theta_{sh}$ is the rms phasor of the converter's sinusoidal current. Observe that the instantaneous three-phase power is the same as the average power for a balanced system.

For the series branch, the three-phase instantaneous power flowing into the series converter under fundamental frequency, balanced conditions is represented by

$$p_{se} = 3\ V I_l \cos(\delta - \theta_l) \tag{3}$$

where $I_l\angle\theta_l$ is the rms phasor value of the ac line current i_l, and $V\angle\delta = V_k\angle\delta_k - V_m\angle\delta_m$ is the rms phasor of the series converter's output voltage v.

It is important to point out that these phasors are defined with respect to the system reference; however, in the actual implementation of the UPFC controller, the converter sinusoidal voltage v_{ish} is typically referred to the controller shunt or sending-end bus voltage v_k, i.e.,

$$\begin{aligned} v_k &= \sqrt{2}\ V_k\ \sin(\omega t + \delta_k) \\ v_{i_{sh}} &= \sqrt{2}\ V_{i_{sh}} \sin(\omega t + \underbrace{\delta_k + \Delta\alpha}_{\alpha}) \end{aligned} \tag{4}$$

For the series phasor voltage, the controls are designed in this paper assuming that vise is synchronized with respect to the receiving-end bus voltage v_l, i.e.,

$$\begin{aligned} v_l &= \sqrt{2}\ V_l\ \sin(\omega t + \delta_l) \\ v_{i_{se}} &= \sqrt{2}\ V_{i_{se}} \sin(\omega t + \underbrace{\delta_l + \Delta\beta}_{\beta}) \end{aligned} \tag{5}$$

These facts must be kept in mind when implementing the controls of the UPFC, as discussed in the next section, and when implementing the corresponding model in any simulation program.

AC losses, which are basically the result of switching losses, can be approximately modeled using series resistors R_{sh} and R_{se} in both converters, and dc losses may be represented with a resistor $R_C = 1/G_C$ connected in shunt with the dc capacitor. These losses have been typically ignored in previous proposed models for the UPFC; however, these resistors are indispensable to have the stability model reproduce the actual behavior of the detailed model. In this case, the UPFC power balance equation (1), assuming real power flow from the shunt converter to the series converter, may be given by

$$\begin{aligned} p_{sh} - p_{se} &= V_{dc} \underbrace{\left(C \frac{\mathrm{d}V_{dc}}{\mathrm{d}t} \right)}_{I_{dc}} + V_{dc}^2 G_C \\ &\quad + 3 \left(a_{sh} I_{sh} \right)^2 R_{sh} + 3 \left(a_{se} I_{se} \right)^2 R_{se} \end{aligned} \tag{6}$$

where a_{sh} and a_{se} are the shunt and series transformers voltage ratios, and V_{dc} is the average dc capacitor voltage. Hence, from equations (2), (3) and (6), it follows that the UPFC dc voltage V_{dc} in the transient stability model can be defined by the following nonlinear differential equation:

$$\begin{aligned} \frac{\mathrm{d}V_{dc}}{\mathrm{d}t} &= 3 \frac{V_k I_{sh}}{C V_{dc}} \cos(\delta_k - \theta_{sh}) - 3 \frac{V I_l}{C V_{dc}} \cos(\delta - \theta_l) \\ &\quad - \frac{G_C}{C} V_{dc} - 3 \frac{a_{sh}^2 I_{sh}^2}{C V_{dc}} R_{sh} - 3 \frac{a_{se}^2 I_l^2}{C V_{dc}} R_{se} \end{aligned} \tag{7}$$

Equation (7) can be significantly simplified if the ac losses represented by R_{sh} and R_{se} are neglected; however, this introduces errors in the model, especially for PWM control, given the "high" ac switching losses. In this case, the equation can be readily transformed into

$$\begin{aligned} \frac{\mathrm{d}V_{dc}}{\mathrm{d}t} &= 3 \frac{V_k k_{sh}}{C a_{sh} X_{sh}} \sin(\delta_k - \alpha) \\ &\quad - 3 \frac{V k_{se}}{C a_{se} X_{se}} \sin(\delta - \beta) - \frac{G_C}{C} V_{dc} \end{aligned} \tag{8}$$

Here, k_{sh} and k_{se} are defined based on a Fourier analysis of the converters' output voltages v_{ish} and v_{ise}, respectively. Since V_{ish} and V_{ise} are the corresponding rms values, these can be expressed as

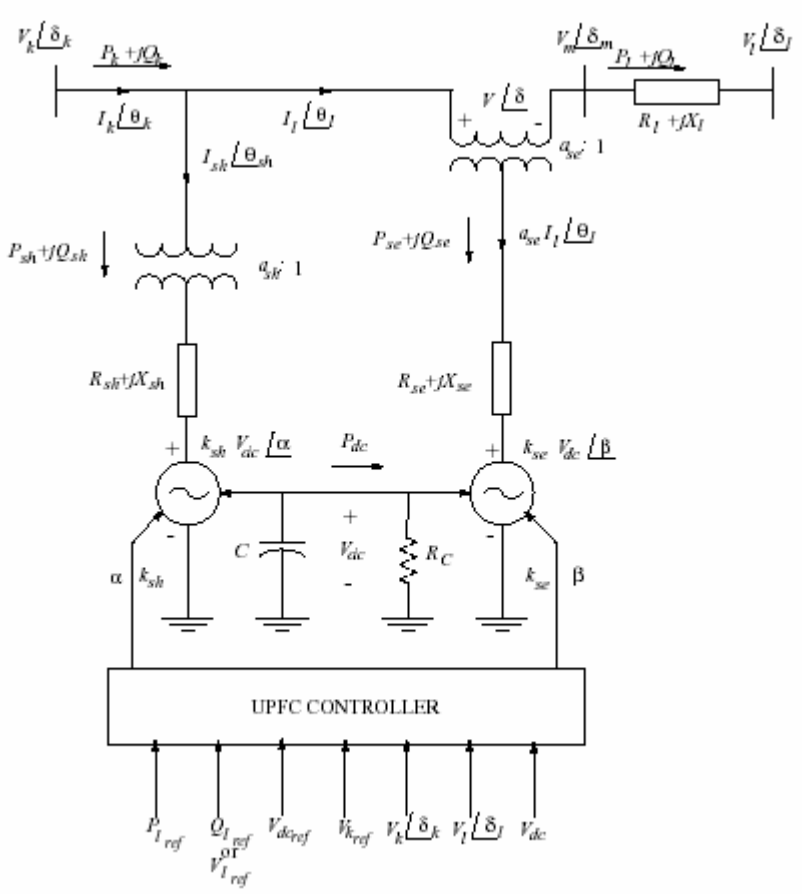
$$V_{i_{sh}} = \frac{1}{2\sqrt{2}} m_{sh} V_{dc} = k_{sh} V_{dc} \tag{9}$$

$$V_{i_{sh}} = \frac{1}{2\sqrt{2}} m_{sh} V_{dc} = k_{sh} V_{dc} \tag{10}$$

where m_{sh} and m_{se} represent the amplitude modulation indices in PWM control of the shunt and series converters, respectively.

Based on equations (7), (9) and (10), the transient stability model of Figure 2, including the controls, which are discussed in detail in the next section, can be represented by the following p.u. set of equations that can be readily introduced in any simulation program:

Figure 2 Transient stability model of the UPFC.



$$
\begin{aligned}
\begin{bmatrix} \dot{x}_{c_1} \\ \dot{x}_{c_2} \end{bmatrix} &= f(x_{c_1}, \alpha, \beta, m_{sh}, m_{se}, V_k, \\
&\qquad V_l, V_{dc}, V, \delta_k, \delta_l, u) \\
\dot{V}_{dc} &= \frac{V_k\, I_{sh}}{C\, V_{dc}} \cos(\delta_k - \theta_{sh}) + \frac{V\, I_l}{C\, V_{dc}} \cos(\delta - \theta_l) \\
&\quad - \frac{G_C}{C}\, V_{dc} - \frac{R_{sh}}{C}\, \frac{I_{sh}^2}{V_{dc}} - \frac{R_{se}}{C}\, \frac{I_l^2}{V_{dc}}
\end{aligned}
$$

$$
0 = \underbrace{\begin{bmatrix}
P_{sh} - V_k\, I_{sh}\, \cos(\delta_k - \theta_{sh}) \\
Q_{sh} - V_k\, I_{sh}\, \sin(\delta_k - \theta_{sh}) \\
P_{sh} - V_k^2\, G_{sh} + k_{sh}\, V_{dc}\, V_k\, G_{sh}\, \cos(\delta_k - \alpha) + k_{sh}\, V_{dc}\, V_k\, B_{sh}\, \sin(\delta_k - \alpha) \\
Q_{sh} + V_k^2\, B_{sh} - k_{sh}\, V_{dc}\, V_k\, B_{sh}\, \cos(\delta_k - \alpha) + k_{sh}\, V_{dc}\, V_k\, G_{sh}\, \sin(\delta_k - \alpha)
\end{bmatrix}}_{g_{sh}(\alpha, k_{sh}, V_k, V_{dc}, \delta_k, I_{sh}, \theta_{sh}, P_{sh}, Q_{sh})}
$$

$$
0 = \underbrace{\begin{bmatrix}
P_k - P_{sh} - V_k\, I_l\, \cos(\delta_k - \theta_l) \\
Q_k - Q_{sh} - V_k\, I_l\, \sin(\delta_k - \theta_l) \\
P_l - V_m\, I_l\, \cos(\delta_m - \theta_l) \\
Q_l - V_m\, I_l\, \sin(\delta_m - \theta_l) \\
P_k - P_l - P_{sh} - P_{se} \\
Q_k - Q_l - Q_{sh} - Q_{se} \\
P_{se} - V^2\, G_{se} + k_{se}\, V_{dc}\, V\, G_{se} \cos(\delta - \beta) + k_{se}\, V_{dc}\, V\, B_{se} \sin(\delta - \beta) \\
Q_{se} + V^2\, B_{se} - k_{se}\, V_{dc}\, V\, B_{se} \cos(\delta - \beta) + k_{se}\, V_{dc}\, V\, G_{se} \sin(\delta - \beta)
\end{bmatrix}}_{\begin{array}{c} g_{se}(\beta, k_{se}, V_{dc}, V_k, V_l, V, \delta_k, \delta_l, \delta, I_l, \theta_l, \\ P_k, P_l, P_{sh}, P_{se}, Q_k, Q_l, Q_{sh}, Q_{se}) \end{array}}
$$

$$
0 = \underbrace{\begin{bmatrix}
I_k\, \cos(\theta_k) - I_{sh}\, \cos(\theta_{sh}) - I_l\, \cos(\theta_l) \\
I_k\, \sin(\theta_k) - I_{sh}\, \sin(\theta_{sh}) - I_l\, \sin(\theta_l) \\
P_k - V_k\, I_k\, \cos(\delta_k - \theta_k) \\
Q_k - V_k\, I_k\, \sin(\delta_k - \theta_k)
\end{bmatrix}}_{g_{con}(V_k, \delta_k, I_k, I_{sh}, I_l, \theta_k, \theta_{sh}, \theta_l, P_k, Q_k)}
\tag{11}
$$

Most of these variables have been previously defined and are clearly depicted in Figure 2. The admittances are defined as $G + jB = (R + jX)^{-1}$, for both converters. The control

system variables are represented here by x_{c1}, which stands for the internal control variables (e.g., $\Delta\alpha$ in Figure 6), and by x_{c2}, which represents the system variables already defined and that are affected by the control (e.g., V_k in Figure 6); these variables change depending on the type of control used. The variable u represents the set points of the controller, which in the case of Figure 2 are $u = [P_{lref}\ Q_{lref}(V_{lref})\ V_{kref}\ V_{dcref}]^T$. Finally, the control system equations are represented here by $f(\cdot)$, which may be linear or nonlinear depending on the type of controls used on the converters.

The UPFC stability model proposed here was also simulated in the EMTP to compare its behavior with respect to the detailed model, illustrating the response to changes in the control orders and sudden changes in the power system (e.g., 3-phase faults) for both models. The shunt and series connected transformers are modeled in the same manner for both the detailed and stability models, i.e., they are lossless and saturation free. The dc voltage V_{dc} was represented through its differential equation (8), which includes the resistor R_C and the capacitance C, which are not physically included in the model but just represented in the equation. The instantaneous voltages v_k and v_l at the shunt and series terminals of the UPFC are traced with the help of a fundamental frequency voltage tracking system, so that the VSCs can be represented in the EMTP using controllable voltage sources based on equations (4) and (5), respectively. The amplitudes of the voltage sources are calculated using (4) and (5). The voltage phase angles α and β come into the model as an output of the UPFC control blocks and are calculated within TACS; the same applies to the amplitude modulation indices m_{sh} and m_{se} for both shunt and series converters.

2.3 Steady State Model

The steady state model can be obtained from the transient stability model of equations (11) and the corresponding controls, which are discussed at length in the next section, resulting in the following set of equations:

$$
0 = \begin{bmatrix}
V_k - V_{k_{ref}} \\
V_{dc} - V_{dc_{ref}} \\
P_l - P_{l_{ref}} \\
Q_l - Q_{l_{ref}} \qquad (V_l - V_{l_{ref}}) \\
P_{sh} - P_{se} - G_C\, V_{dc}^2 - R_{sh}\, I_{sh}^2 - R_{se}\, I_l^2 \\
g_{sh}(\alpha, k_{sh}, V_k, V_{dc}, \delta_k, I_{sh}, \theta_{sh}, P_{sh}, Q_{sh}) \\
g_{se}(\beta, k_{se}, V_{dc}, V_k, V_l, V, \delta_k, \delta_l, \delta, I_l, \theta_l, \\
\quad P_k, P_l, P_{sh}, P_{se}, Q_k, Q_l, Q_{sh}, Q_{se}) \\
g_{con}(V_k, \delta_k, I_k, I_{sh}, I_l, \theta_k, \theta_{sh}, \theta_l, P_k, Q_k)
\end{bmatrix} \tag{12}
$$

Observe that control droops can be readily introduced into these equations [25]. For example, to introduce a typical STATCOM type steady state voltage control variation, the first equation in (12) can be replaced by

$$V_k - V_{k_{ref}} \pm X_{SL} I_{sh} \tag{13}$$

where X_{SL} represents the control droop in p.u. (typically 2-3%).

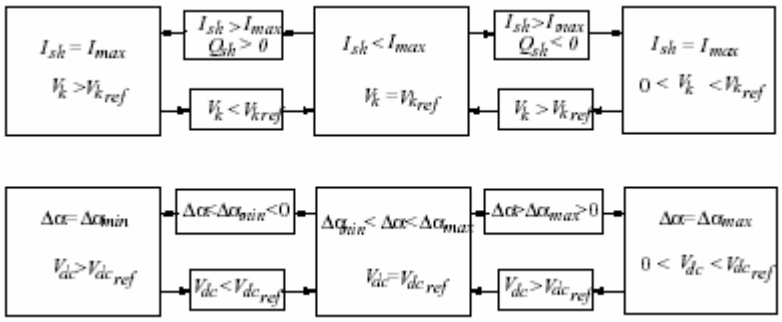
It is important to properly model the controller limits to obtain reliable results in steady state studies by considering the actual current limits in both converters, which are the main limiting factor in VSC-based FACTS controllers [25]. Also other physical system limits such as limits on the power transferred by the device and the series voltage V need to be accounted for, in that they constrain the control capabilities of the UPFC, as discussed in [19]. Besides the actual physical limits, the relationships among the different variables as well as the available variables and equations of the particular model have to be addressed, so that a consistent and hence solvable set of equations is available. Thus, considering that the controls of the shunt and series converters are basically decoupled, when a limit is reached in a variable in one of the converters, another variable corresponding to the same converter has to be released for consistency of the nonlinear set of equations.

For the shunt converter, which controls the sending-end voltage V_k and the dc voltage V_{dc}, if a current limit is reached, only one variable, V_k or V_{dc}, can be released from the set of equations (12), otherwise there is no steady state solution, which is clearly inconsistent with the actual controller operation. Thus, assuming and that resistive losses are small in the proposed model, the following p.u. relationships can be readily obtained:

$$\begin{aligned} P_{sh} &\approx -\frac{k_{sh} V_{dc} V_k}{X_{sh}} \sin(\Delta\alpha) \\ I_{sh} &\approx \sqrt{\frac{k_{sh}^2 V_{dc}^2 - V_k^2}{X_{sh}^2} + \frac{2}{X_{sh}} Q_{sh}} \end{aligned} \tag{14}$$

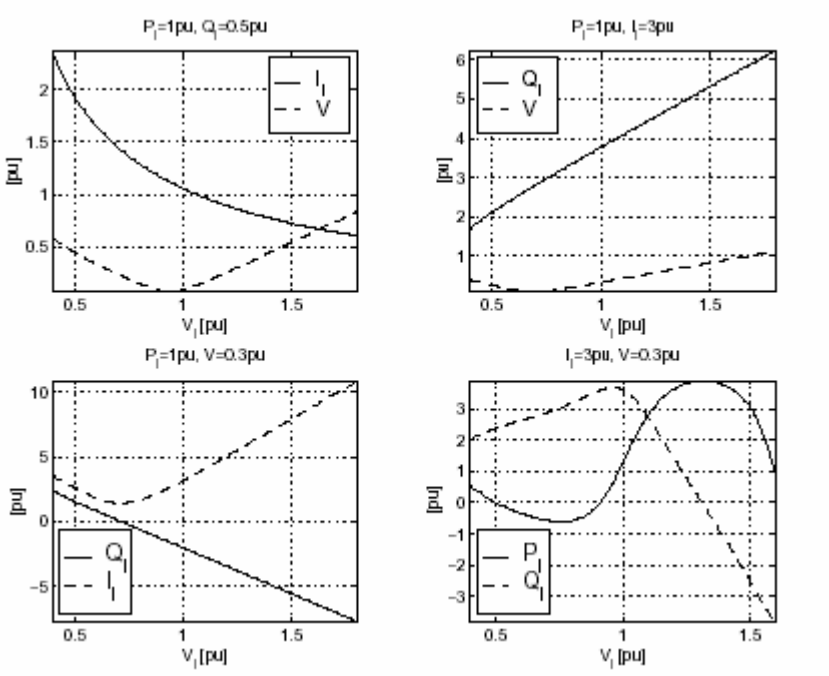
This basically indicates that, under usual steady state, normal operating conditions, where ac voltages are around their nominal values, i.e., about 1 p.u., $P_{sh} \approx -\sin(\Delta\alpha)/X_{sh}$ and $I_{sh} \approx (2\ Q_{sh}/X_{sh})^{1/2}$. Hence, the converter current I_{sh} is strongly coupled to the reactive power flow and hence the bus voltage magnitude V_k, whereas the controller's power transfer capabilities and hence the dc voltage V_{dc} are directly influenced by the phase shift $\Delta\alpha$, as this variable basically defines the power flow and thus the charging and discharging of the capacitor. Therefore, the switching strategies depicted in Figure 3 can be defined, where if a limit is reached, the corresponding variable is fixed and the associated variable is released. For example, if current Ish reaches its maximum limit, equation $V_k - V_{kref} = 0$ is replace by $I_{sh} - I_{shmax} = 0$ in (12). When a given variable recovers, control over the corresponding associated variable is regained; for example, when the voltage V_k is back within the controlling range, i.e., V_k reaches the value of V_{kref}, the converter regains voltage control ($V_k - V_{kref} = 0$) and the current I_{sh} is again allowed to change. It is important to allow the controller to recover realistically from limit conditions. The recovery logic is directly associated with the way the different controlled and controlling variables behave at their limits and after these are applied, which is straightforward in the case of the shunt converter, but significantly more complex in the case of the series converter, as discussed below.

Figure 3 Handling of limits for the UPFC shunt converter in the steady state model.



The relationships among the different variables are different for the shunt than for the series converter, given the fact that both series converter voltage and current are strongly associated with both controlled variables of the device, i.e., P_l and Q_l (or V_l). In [19], this issue is discussed at length, assuming that the terminal voltages of the line to which the UPFC is connected do not change. However, this is not necessarily always the case; in that the receiving-end bus would typically be weaker than the sending-end bus, and may require some reactive support that can be supplied by the UPFC. To explain how the different control and controlling variables and limits interact as V_l changes, a series of plots are used here, illustrating how all of these variables vary. Assuming that the basic limits on the series converter are on the line current I_l and the series injected voltage V, based on the same typical p.u. values proposed in [19] (i.e., a constant sending-end voltage $V_k\angle\delta_k = 1.015\angle 10^o$, $Z_l = 0.01 + j0.1$, and a constant $\delta_l = 0$), equations (12) can be used to obtain the plots shown in Figure 4, for which the following observations can be made:

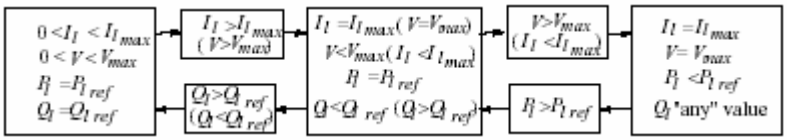
Figure 4 Relationship between different steady state variables on the series converter as the receiving-end bus voltage changes.



- For typical controlled power flow values of $P_l = 1$ and $Q_l = 0.5$, the line current I_l increases as V_l decreases, whereas the series injected voltage V generally increases as V_l deviates from its approximate 1 p.u. value.
- If I_l is limited and P_l is controlled, Q_l decreases as V_l decreases, whereas V tends to decrease or increase for a small decrease or increase of V_l around 1 p.u., respectively.
- If V is now limited and P_l is controlled, Q_l increases as V_l decreases, whereas I_l tends also to decrease or increase for a corresponding decrease or increase of V_l around 1 p.u.
- Finally, for limits on I_l and V_l, P_l decreases or increases for a decrease or increase, respectively, of V_l around 1p.u., whereas Q_l decreases for the same type of variations in V_l.

Since the main task of the series converter is to regulate the active power flow, if one of the two variables I_l or V reaches a limit, P_l is controlled while Q_l is set by the corresponding limits. The limit handling strategy depicted in Figure 5 may be implemented for a decrease in voltage V_l; for voltage increases exactly the opposite strategy should be implemented.

Figure 5 Handling of limits for the UPFC series converter in the steady state model.



Finally, the modulation indices m_{sh} and m_{se} are kept below one p.u. to prevent overmodulation, which would increase the harmonic content in the output signals [24]. Limits on these variables, and hence k_{sh} and k_{se} in equations (12), can be handled as follows:

- For the shunt converter, if a limit in k_{sh} is reached, ac voltage control is lost and hence V_l is freed to change, as in the case of current limits. The option of transition to phase control mode, by controlling the bus voltage V_k through the phase angle shift $\Delta\alpha$ and freeing the dc voltage, as would be done in a STATCOM is not preferred. It would create problems for the series converter, which relies on having a steady dc voltage to control the active power flow in the line, a more important control function for the UPFC than controlling the sending-end bus voltage.
- For the series converter, limits on k_{se} can be accommodated as limits on the series inserted voltage V, since these two variables are tightly coupled.

This steady state model is currently being implemented in the voltage stability analysis tool UWPFLOW [26].

3 Control of UPFC

Due to the inherent and unique characteristics of the UPFC to independently control active and reactive powers, the control strategies of the controller can vary significantly. However, in most cases, the UPFC will likely be used to control its sending bus voltage magnitude by locally generating or absorbing reactive power, and to control power flows on the transmission line by regulating the magnitude and phase angle of the series injected voltage. This control mode is referred to as Automatic Voltage Control Mode for the shunt converter, and Automatic Power Flow Control Mode for the series converter [6]. In some cases, the series converter in Constant Voltage Mode would be preferred since it is presumed that Automatic Power Flow Mode could make post fault recovery and consequent power oscillations worst, unless the UPFC is equipped with power/frequency oscillation damping control.

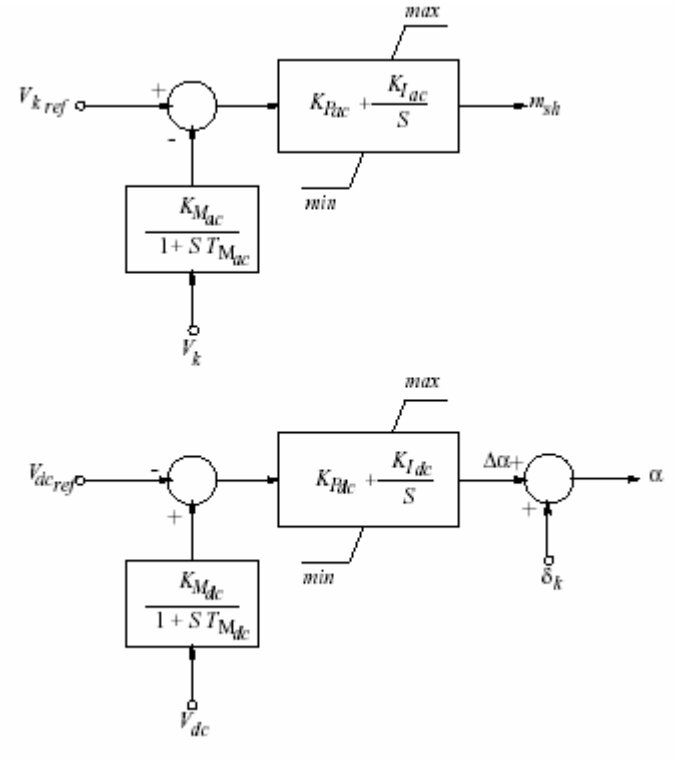
This section concentrates on explaining some of the existent controls that have been proposed to implement the typical UPFC control modes, as well as presenting and justifying some variations to implement other control strategies such as receiving-end voltage control and power/frequency oscillation damping control.

3.1 Shunt Converter Controls

The shunt converter has basically two duties: to control the voltage magnitude V_k at the sending-end bus by generating/absorbing reactive power, and to supply/receive real

power at the dc terminals as demanded by the series converter, which can be achieved by directly controlling the dc voltage V_{dc}. Any excess or deficit of real power at the dc terminals increases or decreases the dc voltage, respectively. The resultant simple and effective shunt converter controller is depicted in Figure 6, and is basically the same as proposed in [13] as a STATCOM control.

Figure 6 Basic shunt branch control of the UPFC.



The shunt converter ac and dc voltages are controlled using two separate PI controllers. The first PI controller directly controls the ac sending-end bus voltage V_k through the modulation index msh, since the output voltage magnitude V ish is directly proportional to the amplitude modulation index msh as shown in (10). The dc voltage, on the other hand, is controlled by the second PI controller that directly varies the phase angle α, as the converter's output voltage is phase-locked to the UPFC sending-end bus voltage v_k. Thus, when $\alpha < \delta_k$ ($\Delta\alpha < 0$), the converter output voltage lags the bus voltage and hence the dc capacitor charges, whereas when $\alpha > \delta_k$ ($\Delta\alpha > 0$), the converter ac voltage leads the bus voltage and hence the capacitor discharges.

The limits on these controls are based on equations (14). Hence, as the current is strongly coupled to the voltages and reactive power flow, its limits define the limits of the first PI controller. However, in this case, the modulation index is typically limited to $0 \leq m_{sh} \leq 1$ to avoid over-modulation, i.e., to reduce the harmonic content in the converter output by operating the converter within the linear region [24]; this imposes additional limits on the controller output.

Limits on the phase angle difference $\Delta\alpha$, which represent limits on the active power transfer capability of the controller as discussed in the previous section, are directly

implemented on the second PI controller. In theory, the phase shift can vary within $-90^o \leq \Delta\alpha \leq 90^o$, corresponding to the maximum active powers that can be transferred by the device as seen in (14). However, converter losses, which introduce a phase shift between the converter output voltage and the ac bus voltage, reduce in practice the range of the phase shift $\Delta\alpha$ variation depending on the characteristics of the converter. For example, for the system and converter used to test the models and controls presented here, the limits chosen for the phase shift are $-25^o \leq \Delta\alpha \leq 25^o$, as these allow for an effective control of the UPFC used in the test system.

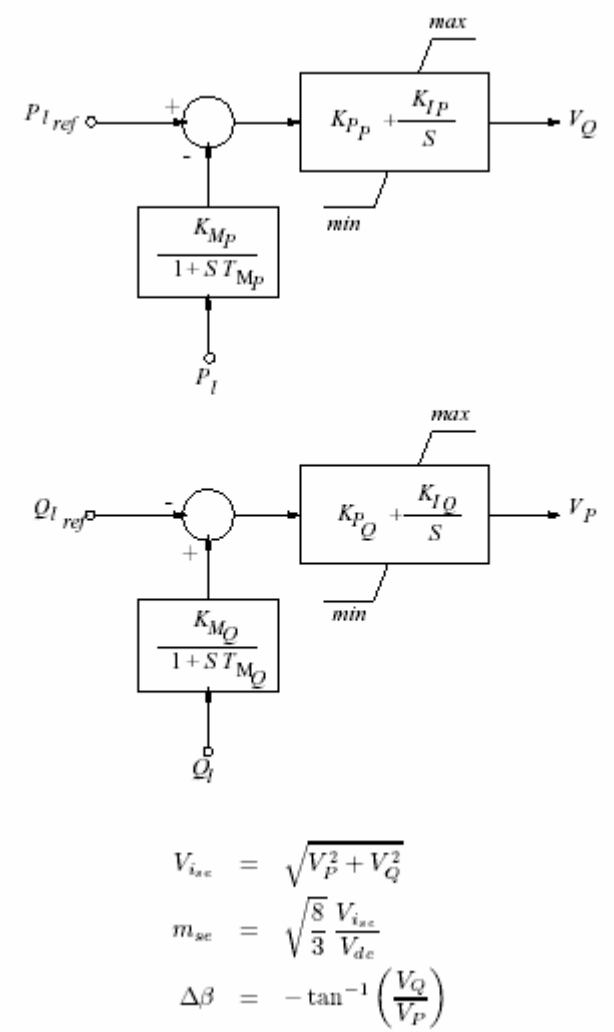
3.2 Series Converter Controls

Two different control schemes for the series converter were implemented and tested to evaluate their performance.

3.2.1 Power and Voltage Control

The first control scheme is a modified version of a control proposed in [19] and is illustrated in Figure 7. In this case, the typical Automatic Power Flow Control Mode for the series converter is slightly modified, as the series converter voltage is varied to control the active power flow on the line P_l, as originally proposed, and to control the receiving-end bus voltage V_l, instead of the typical control of the reactive power flow on the line Q_l. The following assumptions are used in the design of this controller:

Figure 7 Series branch PQ control of UPFC with respect to the receiving-end bus voltage. All variables are in p.u.



1. The receiving-end phasor voltage $V_l\angle\delta_l$ is used as the system reference. Hence, the converter voltage and line current can be decomposed into two components with respect to this phasor, i.e.,

$$\begin{aligned} V_{i_{se}}\angle\beta &= \underbrace{(V_P - jV_Q)}_{V_{i_{se}}\angle\Delta\beta}\, e^{j\delta_l} \\ I_l\angle\theta_l &= (I_P - j\,I_Q)\, e^{j\delta_l} \end{aligned} \tag{15}$$

where the P components are in phase with the receiving-end voltage phasor, whereas the Q components lag 90° this voltage phasor. With this assumption, the active and reactive line powers P_l and Q_l may be approximated, neglecting the line impedance, by

$$\begin{aligned} P_l &\approx V_l I_P \\ Q_l &\approx V_l I_Q \end{aligned} \tag{16}$$

2. Neglecting resistive losses in the line and series converter transformer, the voltage relationships in Figure 2 can be written as

$$V_{i_{se}} \angle \Delta\beta = V_k \angle(\delta_k - \delta_l) - V_l - j \underbrace{(X_l + X_{se})}_{X}(I_P - jI_Q) \tag{17}$$

In typical potential applications of the UPFC, it may be assumed that the line terminal voltages do not significantly change, since the transmission line would connect two large systems. However, it has to be kept in mind that this would not be the case when one of the systems is weak, as in the case of the test system discussed in Section 4, where the UPFC is installed on one of the parallel lines feeding a load, thus making it difficult to properly tune the proposed control. Under this assumption, the following approximate relationships can be readily obtained:

$$\begin{aligned} V_P &\approx A - X\ I_Q \\ V_Q &\approx B - X\ I_P \end{aligned} \tag{18}$$

where A and B are constants representing the real and imaginary parts of $V_k \angle(\delta_k - \delta_l) - V_l$, respectively.
From (16) and (18), one can obtain

$$\begin{aligned} V_P &\approx A - D\ Q_l \\ V_Q &\approx B - D\ P_l \end{aligned} \tag{19}$$

where $D = X/V_l$ is assumed constant. This equation is used to set up the control system for the series converter.

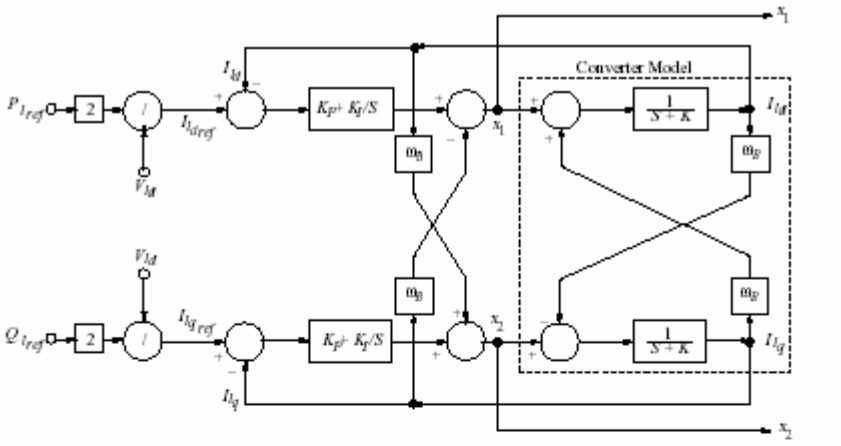
3. Finally, based on the straightforward observation that voltage magnitudes are control variables that are intuitively simpler to define than reactive powers, and that there is a strong coupling between these two variables, the control based on (19) can be modified so that the controlled variable is not the reactive power on the line Q_l but the receiving-end voltage V_l. This final empirical assumption was confirmed by tests run on the EMTP, observing that both reactive power and terminal voltage controllers had a similar performance, as expected.

Choosing limits for these controls is more complex than for the shunt converter. However, the same control limit strategy previously defined for the steady state model of these controls can be applied, i.e., if a converter current or voltage limit is reached, block the control of voltage/reactive power (the second block corresponding to V_P in Figure 7), and control active power until a limit on the other variable is reached. For simplicity, the results presented in this paper were obtained by directly applying limits to the modulation index m_{se} and phase shift angle $\Delta\beta$, which are the basic outputs of these controls.

3.2.2 Active and Reactive dq Control

The second control scheme, proposed in [18] for a dq decomposition of the ac input signals, is directly implemented here. It should be noted that all signals needed for this controller such as sending-end voltage magnitude V_k, receiving-end voltage magnitude V_l, dc voltage V_{dc}, and line current Il are measured and then transformed into a p.u. dq synchronously rotating reference frame; the control signals obtained by this transformation are assumed to be all dc. The control block is depicted in Figure 8.

Figure 8 Series branch dq control of UPFC with respect to the receiving-end bus voltage. All variables are in p.u., and ω_B stands for the fundamental frequency of the system in rad/s.



$$
\begin{aligned}
K &= \frac{R_T\ \omega_B}{X_T} \\
R_T &= R_l + R_{se} \\
X_T &= X_l + X_{se} \\
V_{l_d} &= \sqrt{2}\, V_l \\
V_{k_d} &= \sqrt{2}\, V_k \cos(\delta_l - \delta_k) \\
V_{k_q} &= \sqrt{2}\, V_k \sin(\delta_l - \delta_k) \\
V_{i_{sc_d}} &= V_{k_d} - V_{l_d} - \frac{X_T}{\omega_B}\, x_1 \\
V_{i_{sc_q}} &= V_{k_q} - \frac{X_T}{\omega_B}\, x_2 \\
V_{i_{sc}} &= \frac{1}{\sqrt{2}} \sqrt{V_{i_{sc_d}}^2 + V_{i_{sc_q}}^2} \\
m_{se} &= \sqrt{\frac{8}{3}}\, \frac{V_{i_{sc}}}{V_{dc}} \\
\Delta\beta &= -\tan^{-1}\left(\frac{V_{i_{sc_q}}}{V_{i_{sc_d}}}\right)
\end{aligned}
$$

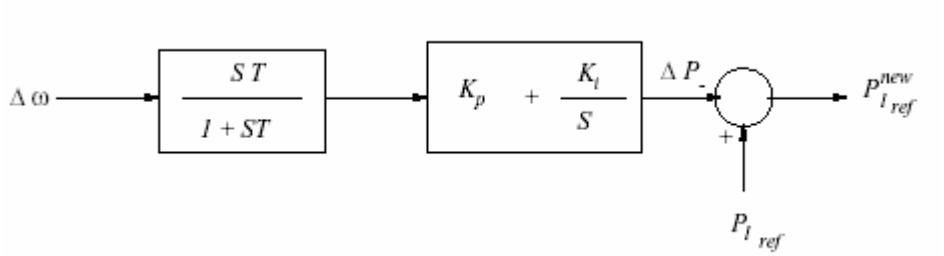
Since this control does not make any major assumptions regarding the behavior of the host system, it is expected to perform better when used in "weak" systems. This is confirmed by the results obtained for the test system discussed in Section 4.

As with the previous controls, a similar logic can be applied here to enforce converter current and voltage limits, keeping in mind that active power control is the main objective of the converter. However, for simplicity in this paper, limits are directly applied to the control outputs m_{se} and $\Delta\beta$.

3.3 Power/Frequency Oscillation Control

Finally, the modulation controller of Figure 9, which was originally proposed in [17], is used to damp power/frequency oscillations. This control directly uses the slip $\Delta\omega$ of any given machine to modify the active power signal reference Pl in any one of the two power controls proposed above for the series converter. The problem with applying this controller in large systems is choosing the most appropriate machine. In practical systems, it is better to use local power or frequency signals to damp oscillations; however, the problem then is whether the controller location is appropriate for having any significant damping of the oscillations [27], considering that the controller location is not typically chosen with this sole objective in mind.

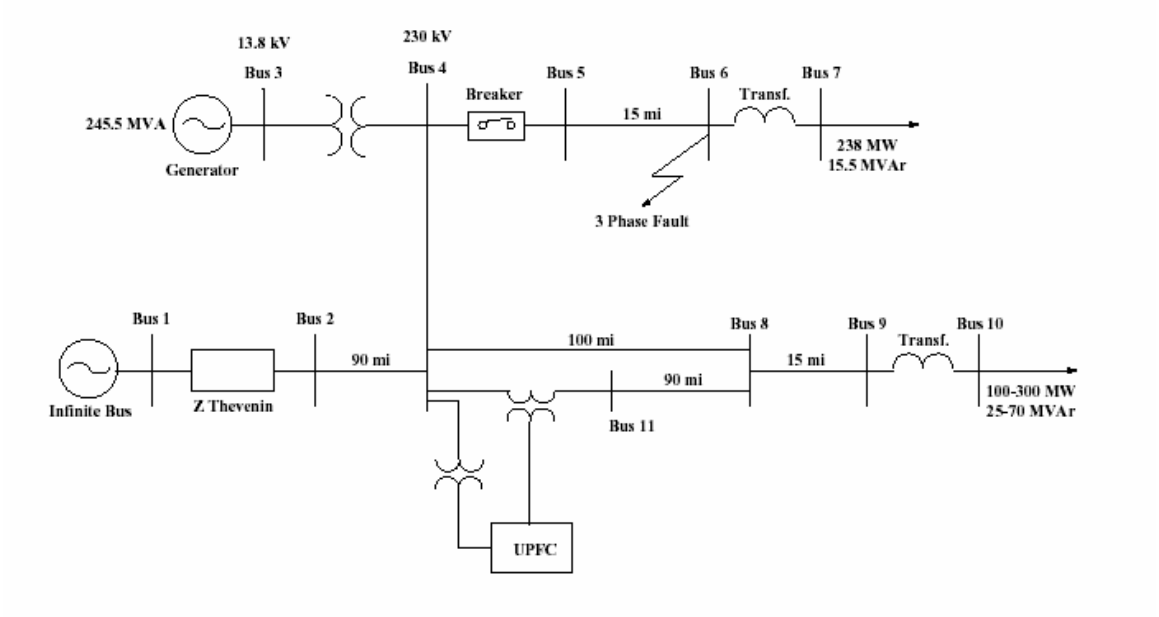
Figure 9 Power modulation control.



4 Test Results

A test system initially introduced in [23] is modified and used here to validate the proposed UPFC models and controls. The 11-bus test system is shown in Figure 10, and consists of an ideal voltage source behind an equivalent Thevenin impedance, a generator with its AVR, a transmission system modeled using distributed-parameter line models, and impedance loads. The main part of the transmission system is composed of two transmission branches; the lower transmission branch has two parallel ac lines with identical parameters but different length, with the Bus 4–Bus 8 line being slightly longer than the Bus 11–Bus 8 line. In steady state and without the UPFC being present to redirect the power flow, the active power flow is almost equally distributed between the two parallel lines; 150 MW on the Bus 4–Bus 8 line and 165 MW on the Bus 11–Bus 8 line. The voltage magnitudes in the system are within the typical permissible limits of 0.95-1.05 p.u. for all buses.

Figure 10 Test system.



After some EMTP simulations and careful assessment of the UPFC role in the sample system, it was determined that the UPFC would be used to increase the power flow in the Bus 11–Bus 8 line from 165 MW to 315 MW, i.e., almost double it, so that in the case of a fault or an outage of the Bus 4–Bus 8 line, the UPFC would be able to supply for the full load. If the UPFC is considered to have two identical six-pulse converter, the ratings of the shunt and series converters, as well as of the accompanying transformers, should be calculated considering the full load line current needed to supply a 300 MW, 70 Mvar load at nominal voltage, i.e., 773 A. The series inserted voltage is assumed to be 1/3 (33 %) of the power system voltage rating, i.e., the maximum magnitude of the series converter voltage would be 76.67 kV, neglecting the voltage drop on the series transformer leakage reactance X_{se}. This voltage is chosen assuming that it produces a desired line current and a steady state amplitude modulation over 0.8, so that the harmonic content of the output voltage waveforms is kept low. Based on these figures, the rating of the series converter/transformer should be $\sqrt{3}$ 76.67 kV 773 A ≈ 100 MVA, which also defines the rating of the shunt converter/transformer. For the simulations, however, a 200 MVA rating was used to increase the power transfer capabilities of the UPFC and thus avoid problems associated with transfer limits on the controller at full loading conditions during the simulations. Although this would significantly increase converter costs, it simplifies the simulation and comparison processes, which is one of the main goals of this paper. The shunt and series transformer leakage reactances are assumed to be 14.5 %.

The UPFC is located at the beginning of the lower ac parallel line to control the power flow. The power system is subjected to different perturbations to simulate both detailed and transient stability models of the UPFC. Thus, the following cases are studied on the test system:

1. The load at the end of the UPFC branch is increased in three steps until reaching full load. For this test studies, the power-voltage control scheme depicted in Figure 7 is

used to control the series inserted voltage for both detailed and transient stability models.

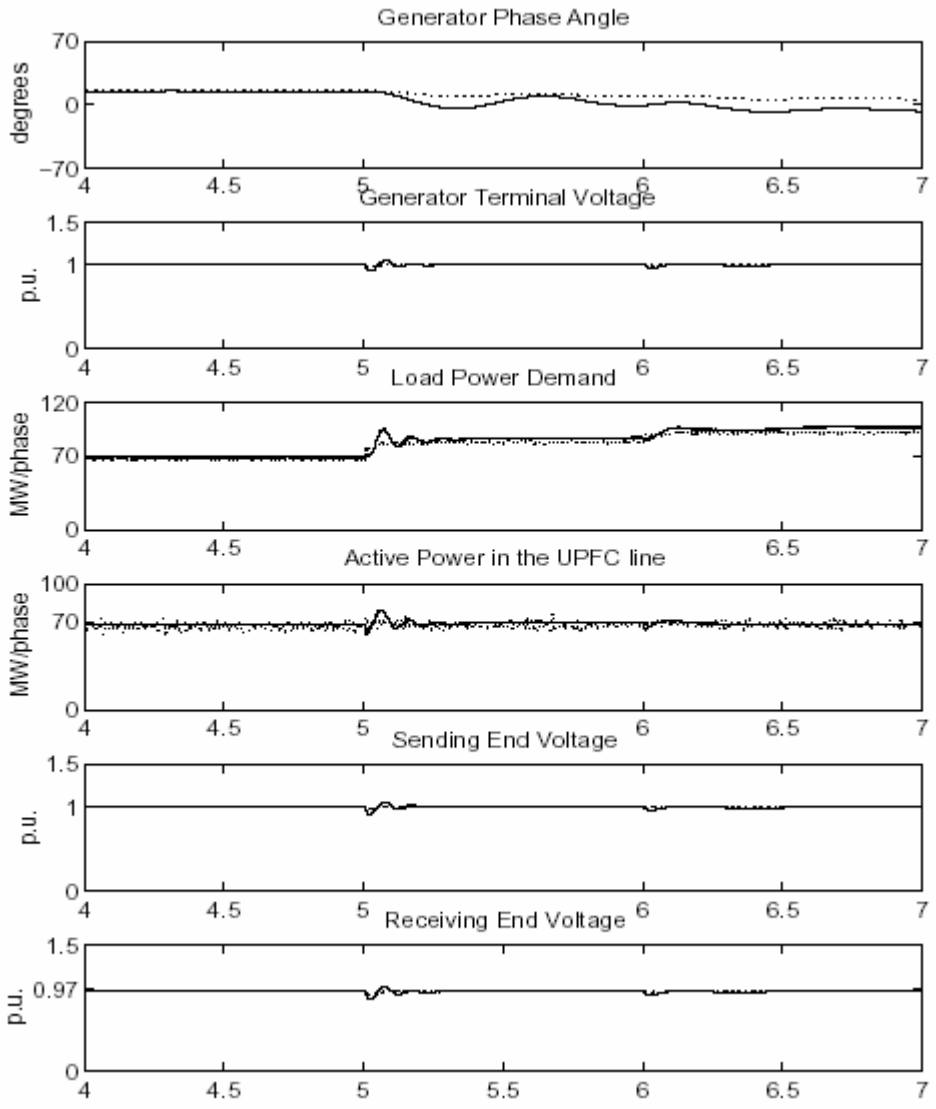
2. A 3-phase fault through an impedance is applied at Bus 6, which is in close proximity to the UPFC. The same proposed control scheme of Figure 7 is used here to control the active power flow in the transmission line and the bus voltage magnitude at the load side.
3. Finally, the UPFC is used to damp oscillations on the generator output power caused by the 3-phase fault at bus 6. The active and reactive power flow in the transmission line was controlled using the control scheme shown in Figure 8.

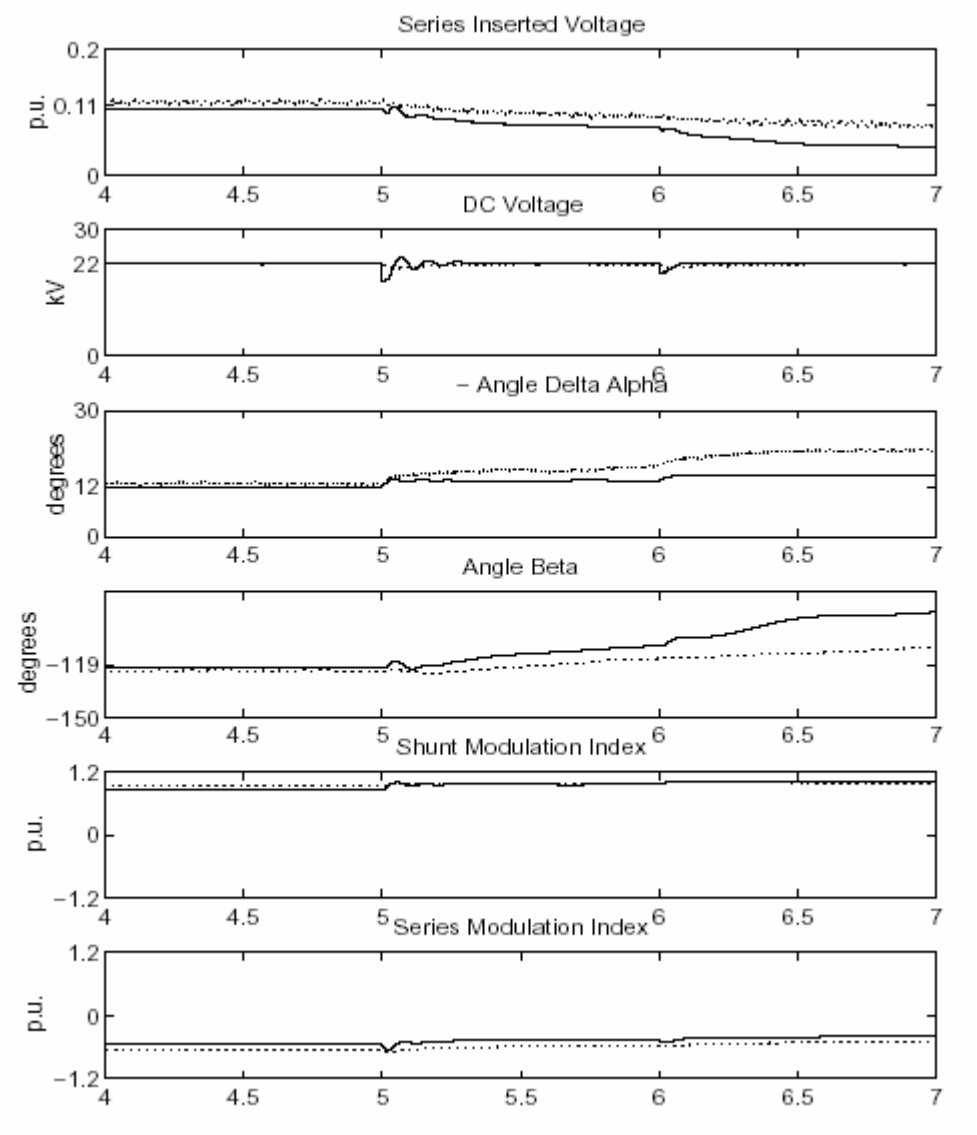
4.1 Variable Load

Load variations at 5 s and 6 s are simulated on Bus 10 to demonstrate the behavior of the UPFC detailed and transient stability models, and to validate the proposed model for small-disturbance stability analysis. The relatively large initial time was chosen to let initial transients die down, so that better comparisons between the two models can be performed, as the start-up processes on both models are fairly distinct due to the significant modeling differences.

The UPFC shunt converter is designed to keep the sending-end voltage at 1.0 p.u., whereas the dc voltage is kept at 22 kV. The series converter varies the magnitude and phase angle of its voltage to maintain the active power on the transmission line at 210 MW, and to keep the voltage magnitude at the receiving-end of the line at 0.97 p.u. The results obtained for both detailed and transient stability models are presented on Figure 11. As it can be observed, there are some differences, although not large, between the models, as is to be expected, since the response of the detailed model cannot be fully captured by the reduced model (similarly for the results shown in Figure 12); however, they both basically present similar trends. It is interesting to notice that the UPFC, due to tight voltage regulation at the sending and receiving-ends, basically works as a phase shifter introducing a series inserted voltage of appropriate magnitude and phase angle between the two ends of the line.

Figure 11 Load variation results for both UPFC models. The continuous line corresponds to the transient stability model, whereas the dotted line corresponds to the detailed model.





To bring closer the responses of both UPFC models, a transfer function $1/(1 + S\,T_c)$ with converter time constant T_c, was introduced in the transient stability model, immediately before the control outputs m_{sh}, $\Delta\alpha$, m_{se} and $\Delta\beta$, to slow down its response. This additional transfer function was necessary due to the rather different time responses of these two models, as there are no delays due to all the switching in the reduced model. Other than that, the control systems for both models are basically the same.

To simplify the calculations needed to set up the transient stability model, all converter losses were concentrated on the dc resistance R_C, and the ac resistors were neglected, i.e., $R_{sh} = R_{se} = 0$, which certainly introduces some minor errors in the simulation. The actual values of these resistors, as well as the reactances X_{sh} and X_{se}, can be computed from the steady state equations (12), based on a steady state point obtained from the detailed simulation. The reactances X_{sh} and X_{se} in the simulations presented here

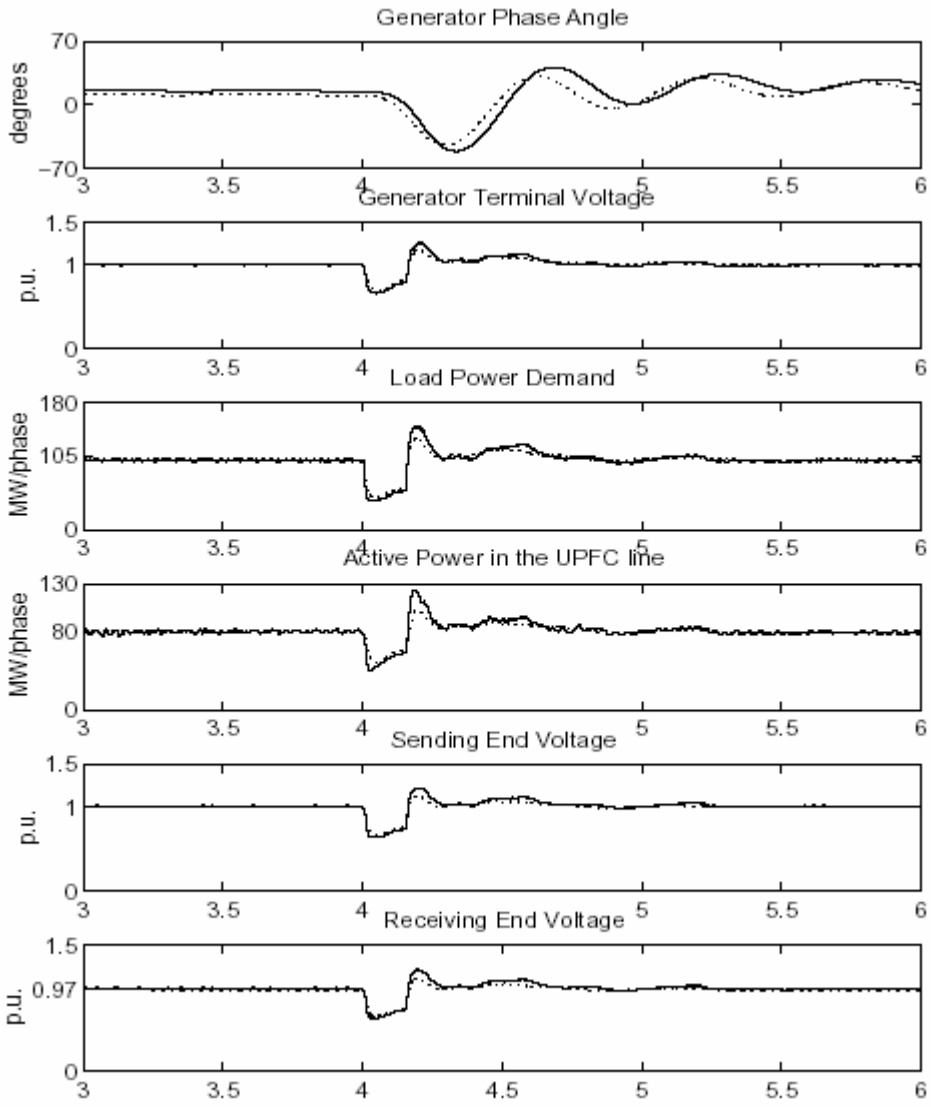
were represented directly by the converter transformers, but these should be computed when implementing the model in a transient stability program. It is important to highlight the fact that converter losses change for different steady state operating points, due to the changing switching conditions of the VSC; hence, it was necessary to compute a different value of R_C for each load step.

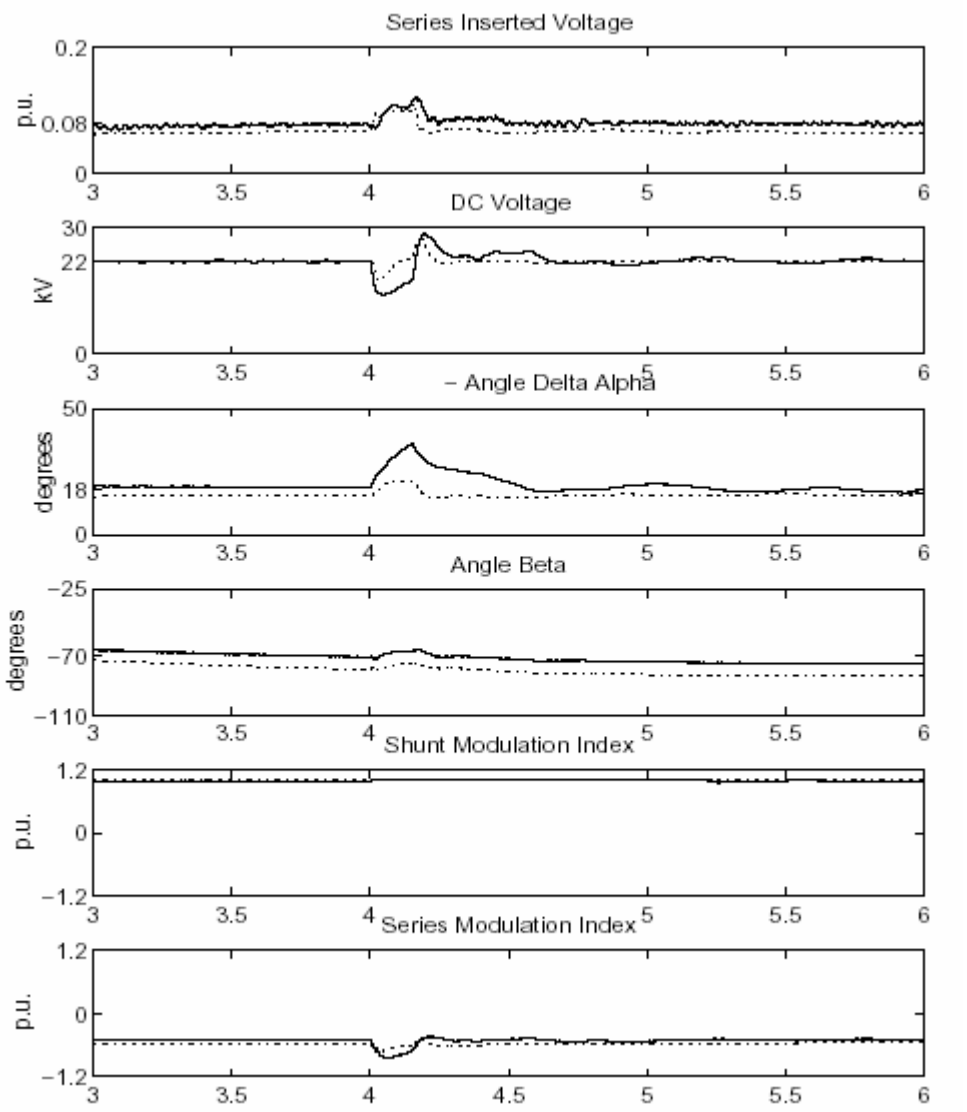
The series converter control used in these simulations was not easy to tune. The main reason for this problem is that this control scheme relies on having strong reactive support on the receiving-end of the line, i.e., a V_l voltage that is not very sensitive to the line flows, as discussed in Section 3, which is clearly not the case in the current test system.

4.2 Three-phase Fault

A 3-phase fault through an impedance is applied at Bus 6 at 4 s for full loading conditions at Bus 10. Nine cycles after the fault, i.e., at 4.15 s, the circuit breaker between Buses 4 and 5 is opened, clearing the fault and disconnecting the load at Bus 7. The generator at bus 3, which has an AVR to keep its terminal voltage at 1.0 p.u., recovers successfully after clearing the fault, as it can be seen on the corresponding waveforms depicted in Figure 12. The series converter continues to control active power flow and voltage magnitudes at the receiving-end voltages using the same control scheme used in the previous simulations. As in the previous study case, the shunt converter maintains the sending-end voltage and the dc voltage at 1.0 p.u. and 22 kV, respectively, while the active power in the transmission line is kept at 240 MW, and the voltage magnitude at the receiving-end at 0.97 p.u. The parallel ac line delivers the rest of the load demand, i.e., 60 MW for a total load power of 300 MW.

Figure 12 Three-phase fault results for both UPFC models. The continuous line corresponds to the transient stability model, whereas the dotted line corresponds to the detailed model.





4.3 Power Oscillation Damping

The Automatic Power Flow Control Mode is changed to a Power Oscillation Damping Control Mode by simply allowing the active power reference to change according to the changes in generator speed, as explained in the previous section. The simulations in this case were carried out using the detailed UPFC model and the dq-based series converter control depicted in Figure 8. The reason for carrying out the studies with the detailed model only is to make sure that the oscillation control capabilities are not affected by any major modeling approximations, and thus test the realistic capabilities of the controller. The change in control structure, on the other hand, is due to the fact that this control shows better performance than that used in the previous two simulations, because it does

not rely on having a constant voltage on the receiving-end of the line, as discussed in Section 3.

The results depicted in Figures 13 and 14 show that, by allowing the UPFC to counteract the changes in the generator output power, the oscillations caused by the 3-phase fault at Bus 6 are quickly controlled. The generator phase angle oscillations are damped faster and, hence, the system appears to be more stable. However, observe that the power oscillations on the lines have actually increased, to compensate for the reduced oscillation in the generator, which creates a problem for the load connected at the end of the corresponding transmission branch.

Figure 13 Fault results for the detailed UPFC model in Automatic Power Flow Control Mode.

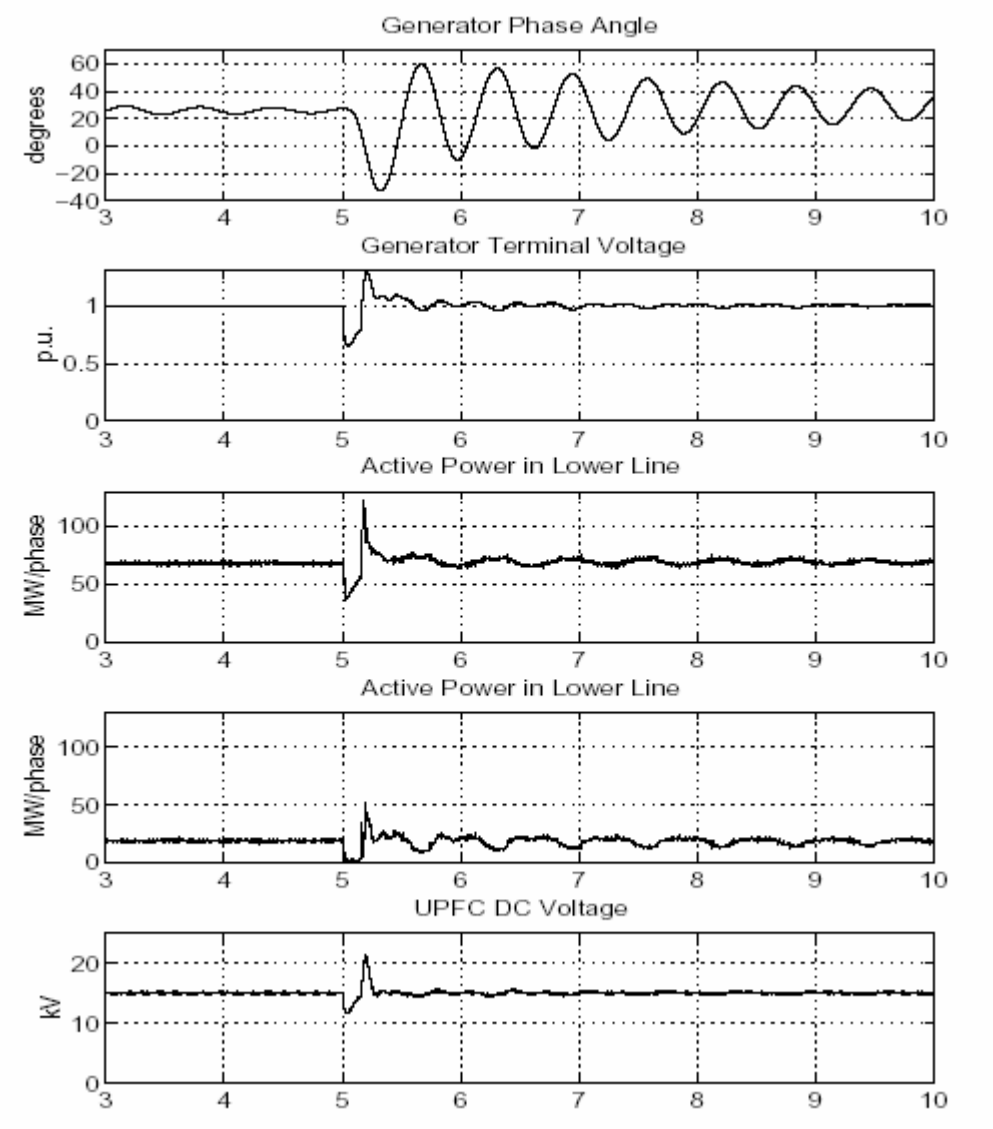
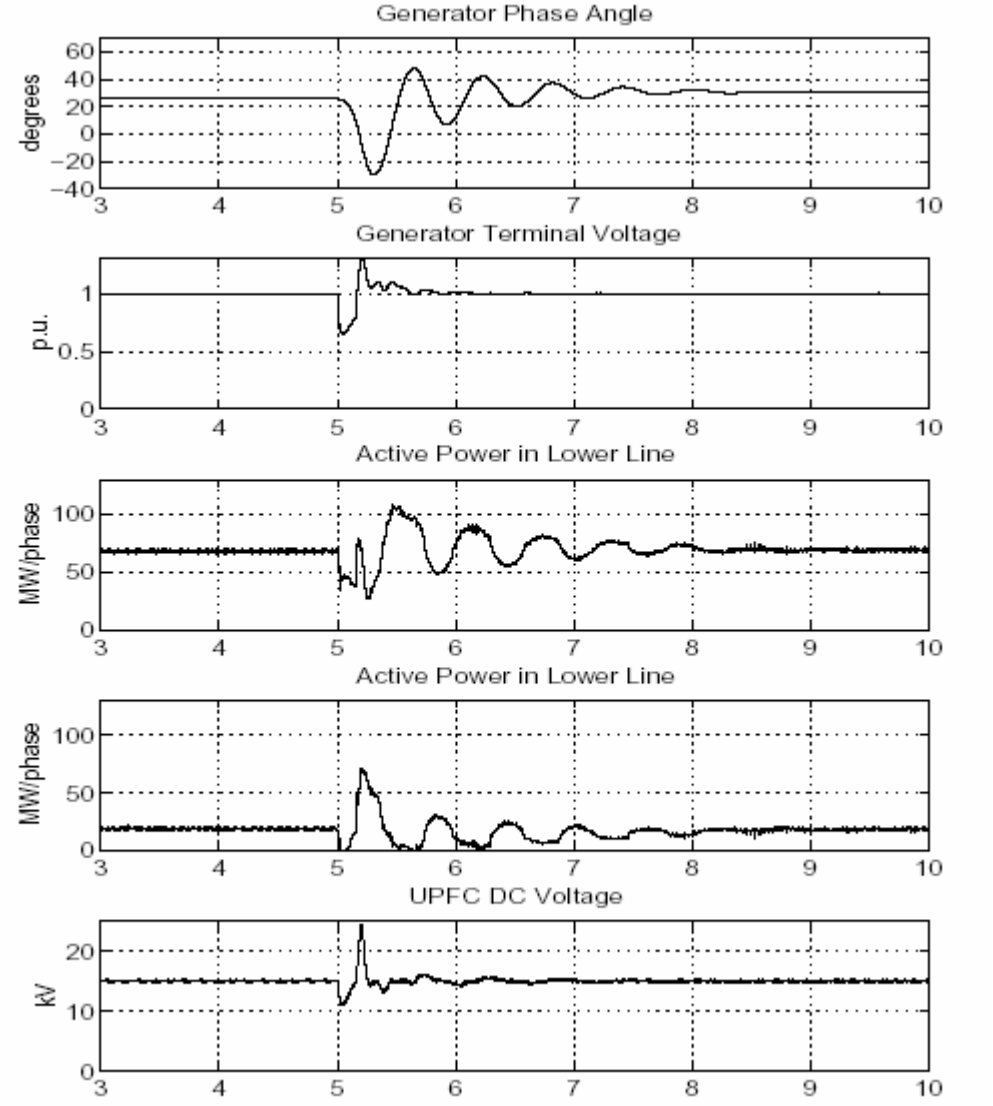


Figure 14 Fault results for the detailed UPFC model in Power Damping Oscillation Control Mode.



5 Conclusions

This paper proposes and fully justifies novel and fairly complete transient stability and steady state models for the UPFC, including a detail description of the proper handling of limits in the controller. The models are successfully validated by obtaining similar results in the EMTP for various operating conditions of a test system for both reduced and detailed models of the controller.

The paper also presents a detailed description of various PWM-based control structures and strategies for the UPFC, comparing qualitatively and quantitatively their performance, determining the advantages and shortcomings of these controls. Novel and simple controls are proposed and analyzed for both UPFC series and shunt converters.

The proposed models can be directly implemented in any software package that has some external programming capabilities, or can be readily integrated in any power flow, voltage stability, and/or transient stability programs, as the authors are currently doing. It should be noted that the model is independent of the type of control used in the UPFC; the results were obtained for a PWM-based control techniques, but other control strategies such as phase angle control can be implemented without any changes to the model.

6 Acknowledgment

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